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43064001 Tokyo '89 ULSI PROCESS TECHNOLOGY SYMPOSIUM in Japanese 7-8 Dec 88 pp I1-V7

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CONTENTS

Physical Limitation of Semiconductor Devices, 0.5~0.3 μm Device Technology

43064001 Tokyo '89 ULSI PROCESS TECHNOLOGY SYMPOSIUM in Japanese 7-8 Dec 88 pp I1-I9

[Article by Hideo Kadonami, Central Laboratory, Hitachi, Ltd.]

[Text] **1. Physical Limitation of Semiconductor Devices**

The higher integration of DRAM devices began in 1970 and has progressed by a factor of four every 3 years since then, as shown in Figure 1. This higher integration has been supported primarily for the miniaturization of devices, which have been reduced by a factor of 10 over the last 15 years, as shown in Figure 2. Along with miniaturization, almost all electrical voltage strength has been lowered. This voltage strength limitation was calculated in 1972 by Hoeneissen and Mead, as shown in Figure 3. This calculation indicates that the purity of substrates must be increased to complement a characteristic deterioration due to the miniaturization of MOS transistors. With this increase, the voltage strength between a substrate and its drain is lowered, limiting further miniaturization.

Then in 1973, the hot carrier phenomenon[1] was discovered, which also made further miniaturization difficult.

As shown in Figure 4, the hot carrier voltage strength BV_{HC} becomes about 2 V lower than the source/drain voltage strength BV_{DS}. As already shown in Figure 1, the 1 gigabit DRAM device of the 21st century will have to use 0.1~0.15 μm transistors. Three or four years ago, 0.3 μm was the miniaturization limit for practical mass production. However, Sai-Halaz achieved practical operation of MOS transistors less than 0.1 μm, as shown in Figure 5.[2] Though such transistors show proper characteristics only at temperatures below 77 K, it has been proven experimentally that their physical operational limit is at least below 0.1 μm.

In view of the subthreshold characteristics, it is desirable that transistors less than 0.2 μm should be operated at a low temperature, for example, 77 K. As shown in Table 1, their speed becomes two to three times greater and the leak current can be disregarded in practice. This means that a DRAM can be regarded as a SRAM, the Al wiring resistance is reduced to one-seventh, and electromigration becomes negligible. However, at 77 K

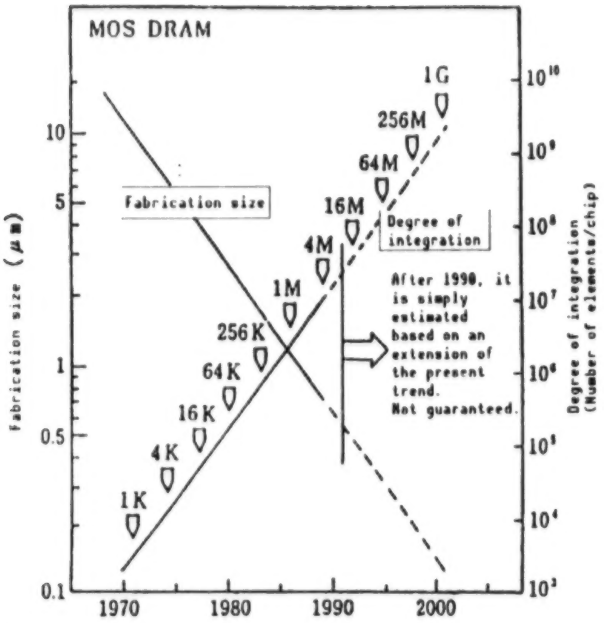


Figure 1. Trend of DRAM Miniaturization

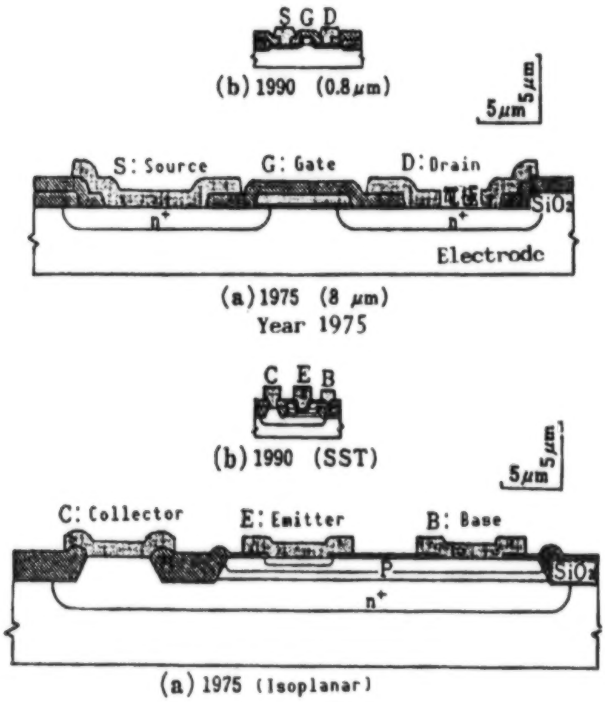


Figure 2. Cross Sections of MOS and Bipolar Transistors in 1975 and 1990

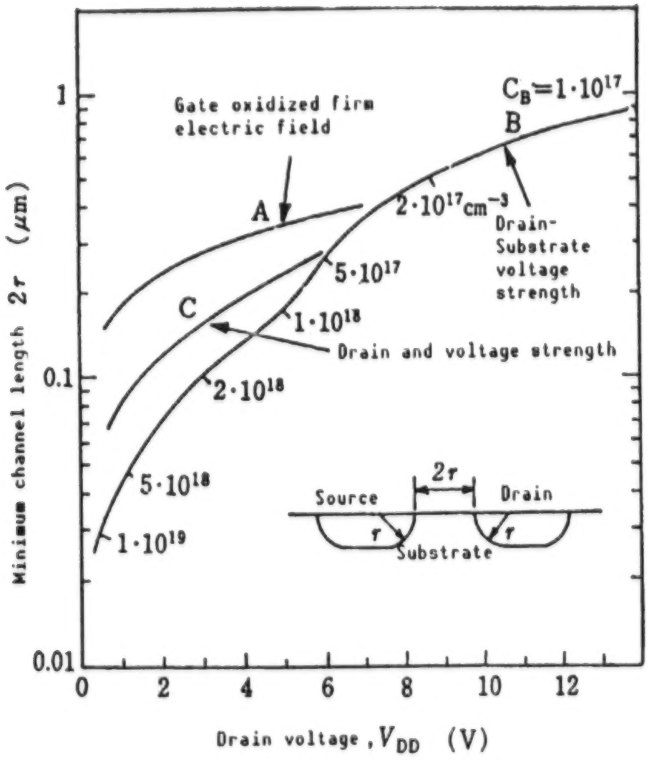


Figure 3. Relationship Between Transistor Minimum Channel Length and Drain Voltage Strength by the Limitation of Connection Voltage Strength and Oxidized Film Electric Field (From Hoeneissen and Mead, © Pergamon Press 1972)

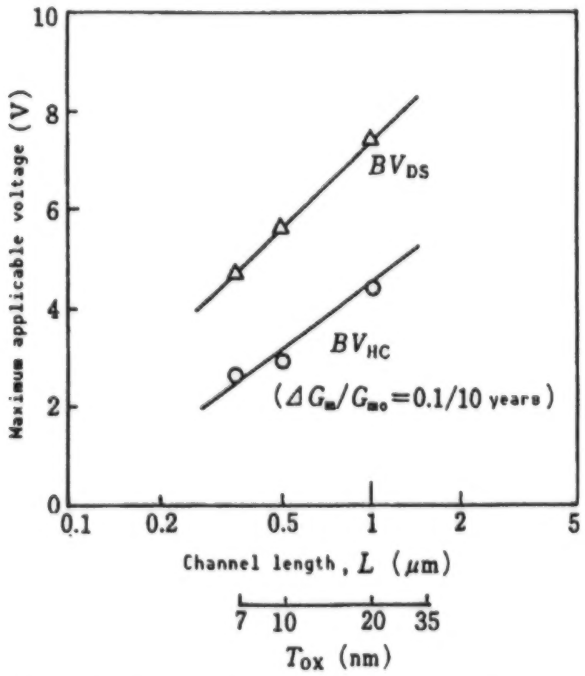
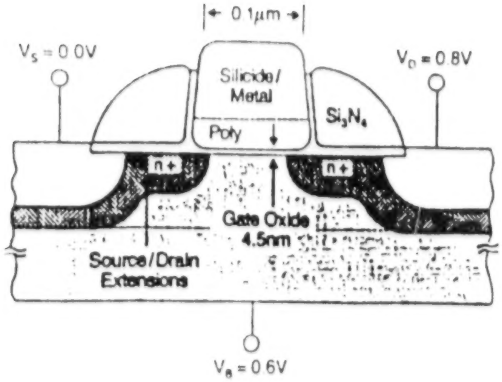
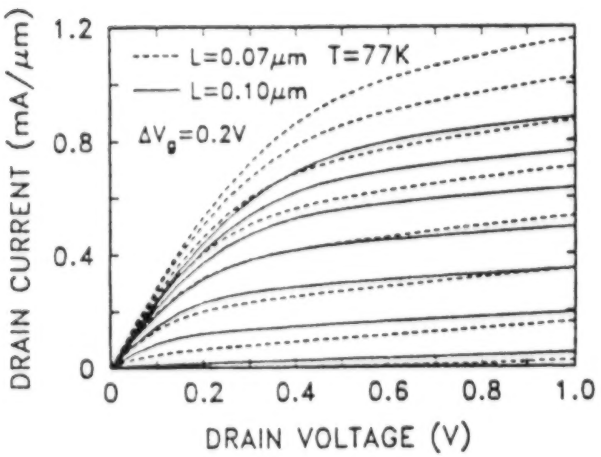


Figure 4. Maximum Applicable Voltage Determined by Hot Carrier Voltage Strength BV_{HC} and Source/Drain Voltage Strength BV_{DS} (From Takeda, et al., © IEEE 1985)



Schematic device cross section and bias levels.



Device terminal characteristics. Maximum V_G is 1.5 V, substrate is biased at 0.6 V. The 0.07 μm device at V_D = 1 V has a maximum g_m of over 940 μS/μm, while the 0.1 μm has 770 μS/μm. The room temperature g_m of these devices with 0 V substrate bias is 590 and 505 μS/μm, respectively.

Figure 5. Cross Section and Id-Vd Characteristics of 0.1 μm MOS Transistor (From Sai-Halasz, © Applied Physics Society 1988)

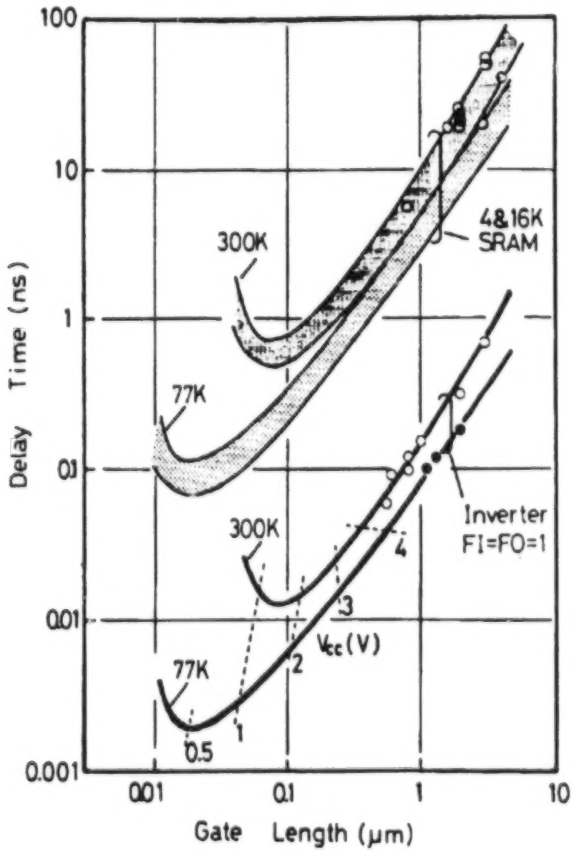
or -50°C, can the ambient temperature environment be applied to machines other than stand-alone mainframe computers? It may be that ease of use will set a limit to the miniaturization of devices.

Meanwhile, miniaturized transistors require a lower voltage and the minimum value must exist in the circuit delay time, as shown in Figure 6. As this minimum gate length value is around 0.1 μm at room temperature, the miniaturized transistor limitation has still to be determined in this respect.

Table 1. Comparison of RT and LN-Cooled CMOS Characteristics

	300 K	77 K
Electron/hole mobility	1	3.5
Saturation velocity	1	1.3
Subthreshold swing	75~80 mV	20~25 mV
Vt limit*	0.55 V	0.25 V
Supply voltage**	2.5~3.3 V	2.5~3.3 V
Junction capacitance	1	0.7
LSI speed	1	2~3
Delay-power product	1	0.33
Al resistance	1	0.14
Latchup base current	1	1,000
Charge holding time	1	10,000 (220 K)

* With 0.15 V Vt variation.
** 0.3~0.5 μm channel length for LDD.



Calculated Delay Time vs. Gate Length

Figure 6. Relationship Between Delay Time and Gate Length of CMOS-SRAM and Invertor (From Masahara, © ECS 1987)

The main theme of this chapter on the "Physical Limitation of Semiconductor Devices" is that this limit may not be around 0.1 μm as extrapolated from conventional practical trends. The physical limitation may be determined by local impurities becoming visible near 0.01 μm below 0. as well as by 1/f noises or quantum effects, etc.

2. 0.5~0.3 μm Device Technology

As already shown in Figure 4, conventional transistors could not be used for 0.5~0.3 μm devices because of their hot carrier voltage strength. As the hot carrier is generated under a high electric field, the most intensified electric field should be lessened. For this purpose, the double diffused drain (DDD), lightly doped drain (LDD), etc.,[4] have been developed, as shown in Figure 7. The LDD has a high design allowance as it masks the side wall spacer to form the n⁻ layer. However, a comparatively high electric field exists below the side wall spacer section, thereby making it possible for hot carriers to jump into the side wall spacer section, thereby lowering its reliability.

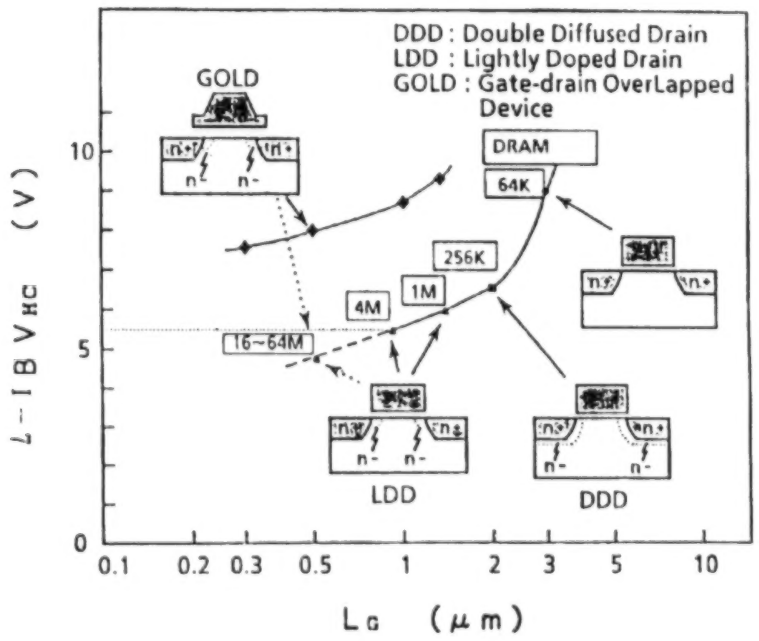


Figure 7. Hot Carrier Voltage Strength of Various MOS Transistor Structures (From Takeda, © IEEE 1988)

To address this problem, the gate-drain overlapped device (GOLD),[5] as shown in Figure 8(a), was developed, and its maximum electric field was reduced, as shown in Figure 8(b). With this device, a considerable improvement has already been attained as shown in Figure 7.

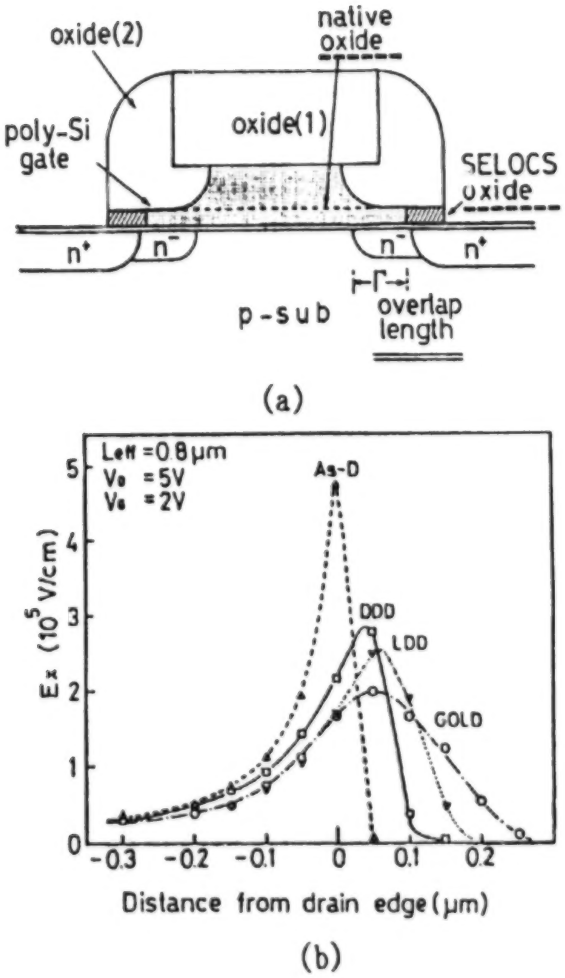


Figure 8. GOLD Transistor Structure
(a) and Electric Field Distribution
(b) of Various MOS Transistors
(From Takeda, © IEEE 1988)

3. 0.5~0.3 μm Process Technology

The process of "0.5 μm age" can almost be viewed as an extension of the "0.8 μm age," as shown in Table 2, but the stepper must be improved. In this respect, the high NA g line (λ = 435 nm) and i line (λ = 365 nm) are competing with each other. However, the latter is winning as good resists for the i line have been recently developed. When the resolution is raised, the depth of focus of a high NA lens becomes shallower. Therefore, to deepen the focus position virtually in the direction of the light axis, the focus latitude enhancement exposure (FLEX) system[6] has been proposed. With three exposures, the depth of ± 1 μm for the first exposure is extended to about ±4 μm, as shown in Figure 9.

Table 2. Transition of MOS Integration Circuit Process Device Technology

Starting time of mass production		1970 Δ	1975 Δ	1980 Δ	1985 Δ	1990 Δ	1995 Δ	2000 Δ
Generation (μm)		12	8	5	3	2	1.3	0.8	0.5	0.3	0.2	0.15
DRAM		1K	4K	16K	64K	256K	1M	4M	16M	64M	256M	1G
Cell	Structure	3T	1T・planer				Layer/Groove shape			Vertical 、SOI		
	Ti(nm)	120	100	50	35	20	10	8	5	4	3	
Device	Power supply voltage	~20V	12				5		(Inside 3.3)	3.3?		
	Transistor	pMOS	nMOS					CMOS			BiCMOS	
	Drain structure	SD				DD		LDD (Improved)		Vertical		
	Tox(nm)	120	100	75	50	35	25	20	15	12	10	8
	Leff(μm)	~8	5	3	2	1.3	0.8	0.8	0.5	0.3	0.2	0.15
	Xj(μm)	~1.5	0.8	0.5	0.35	0.3	0.25	0.2	0.15	0.12	0.1	0.08
Process	Lithography	Close exposure			Reflected projection	1/10 minification	1/5 minification (Excimer) Electron beam X-ray					
	Etching	Solution liquid			Plasma 、RIE				μ wave	Low temperature μ wave (Light assist)		
	Element separation	Planer		LOCOS				(Improved)		Shallow groove	Deep groove	
	Gate metal	Al	Poly Si	2-layer poly Si		Polycide		(Al short circuit)		Hard-to-melt metal		
	Wiring material	Al		Al-Si			Al-Si-Cu (barrier metal)(Superconductivity?)					
	Wafer diameter	2	2.5	3	4	5	6	6~8	8	8~10 inch φ		

Note 1: Even though a clear-cut distinction is supposed to exist between generation devices, some are used over generations and vary between makers.

Note 2: After 0.5 μm technology, it is estimated based on preceding technologies.

The 0.3 μm lithography is called "excimer laser system" and, with technological improvements, a relationship between the high NA g line and the i line may develop into a relationship between the high NA line and the excimer. With the application of contrast enhanced lithography (CEL), the conventional system will still be used more than ever.

Meanwhile, as the thickness of various films does not change as much as in the miniaturization of a plane size, a high aspect ratio pattern has to be formed. To satisfy the contradictory requirement for high anisotropy and high selectivity, a low-temperature dry etching technology has been developed. As shown in Figure 10, this requirement has been met[7] by utilizing a radical reaction with high selectivity while continuing to suppress the side wall reaction at a low temperature.

At this stage, the reliability of miniaturized Al system wiring is now in question. Al-SiCu mixed with Cu has improved the electromigration voltage strength but it is hard for a single-layer material to attain low resistance and high reliability. Thus, a silicide of W and Mo, or a sandwich structure with TiN or TiW are now used.

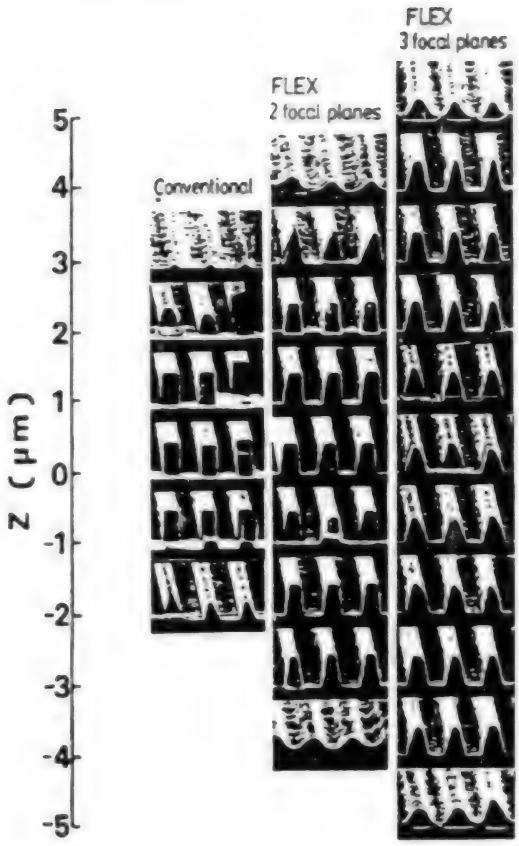


Figure 9. Expansion of Focus Depth by FLEX
(From Fukuda, © IEEE 1987)

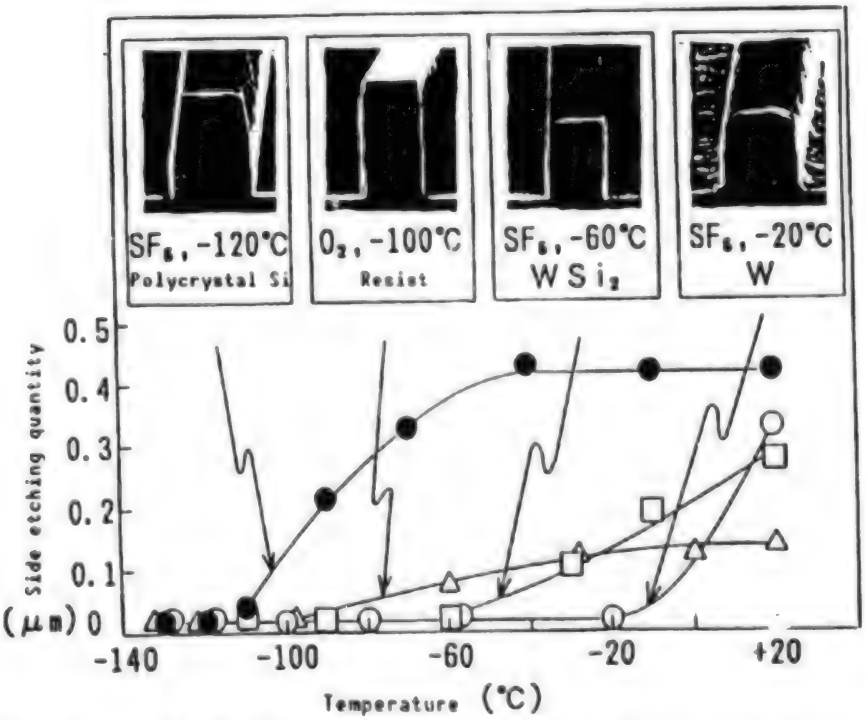


Figure 10. Side Etching Reduction by Low Temperature Etching
(From Taji, © Applied Physics Society 1988)

Further, as the connection hole between wirings becomes narrower, it becomes harder to embed the Al wiring with just an improved version of the conventional sputter method. Therefore, a technology to embed W selectively in the connection hole has been developed. There are two methods for this purpose. One is to grow W only on the Al below the connection hole with a selective growth process, and the other is to embed it with etching after coating it all over. Either way, it is a prerequisite for wiring less than 0.5 μm.

In addition to these, there are many tasks to be solved, such as the reliability of an ultra-thin insulation film and perfect pn connection. Further, for the entire manufacturing process, dust prevention measures, and pollution and damage reduction, which become increasingly problematic as miniaturization progresses, are heaped before us.

4. Future of Semiconductor Devices

It is estimated that conventional methods of miniaturization can be used even at room temperature for devices up to 0.2 or 0.3 μm. For devices in the 0.2~0.1 μm range, a low temperature may be required unless a breakthrough technology is applied. If a memory cell can be structured, this environment period will be realized in the 256M bit age, as shown in Figure 1.

It is hard to predict what will come after that period, but the quantum effect element, tunnel element, etc., which are now being studied hard, may extend the semiconductor integration circuit limitation further. It is estimated, rather, than an element using the granularity of electrons, or an element using the wave property of electrons has to be developed. As a wave property element is generally inferior in drive capability, the logic circuit should be formed with the wave style as it is. I believe a true breakthrough lies in this development.

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0.5~0.3 μm Lithographic Technology (1)--G-Line, I-Line, Excimer Lasers--Problems, Solutions

43064001 Tokyo '89 ULSI PROCESS TECHNOLOGY SYMPOSIUM in Japanese 7-8 Dec 88 pp II1-II20

[Article by Toshiro Tsumori, Sony Corp.]

[Text] **1. Transition of Design Rules**

Design rules have progressed fourfold over the last 2-3 years. A 16M DRAM was announced at the ISCC in 1988, and at the present pace, it is estimated that a 64M DRAM (16M SRAM) will be announced in 1991 or 1992.

Design rules are set in a package that includes the progress of lithographic technology and chip size estimates.

Chip size depends on device structure and design rule; it is estimated it will be 130~140 mm^2 for 16M DRAM devices and about 200 mm^2 for 64M DRAM devices.

Meanwhile, lithography technology is capable of a resolution limit of 0.45 μmL/S for the g-line NA 0.55 class and 0.28 μmL/S for the excimer (248 nm) NA 0.50 class. From the above estimates, it is predicted that future design rules will be 0.6~0.5 μm for the 16M DRAM class and 0.35~0.30 μm for the 64M DRAM class. Mass production of the first generation of 16M DRAMs may begin as early as 1992, and by 1995 or 1996 for the 64M DRAM.

2. Present Status and Measures of 0.5 μm Lithographic Technology

As a target specification, it is necessary to have a resolution of 0.5 μmL/S with a junction accuracy of more than ±0.15 μm. The 0.5 μm lithographic technology may be started with present technology if mass production has to begin in 1992.

The g line or i line could be candidates for a stepper, but the high NA g line may be the primary candidate for the first generation mass production in 1992 in view of its degree of technological completion and the time factor.

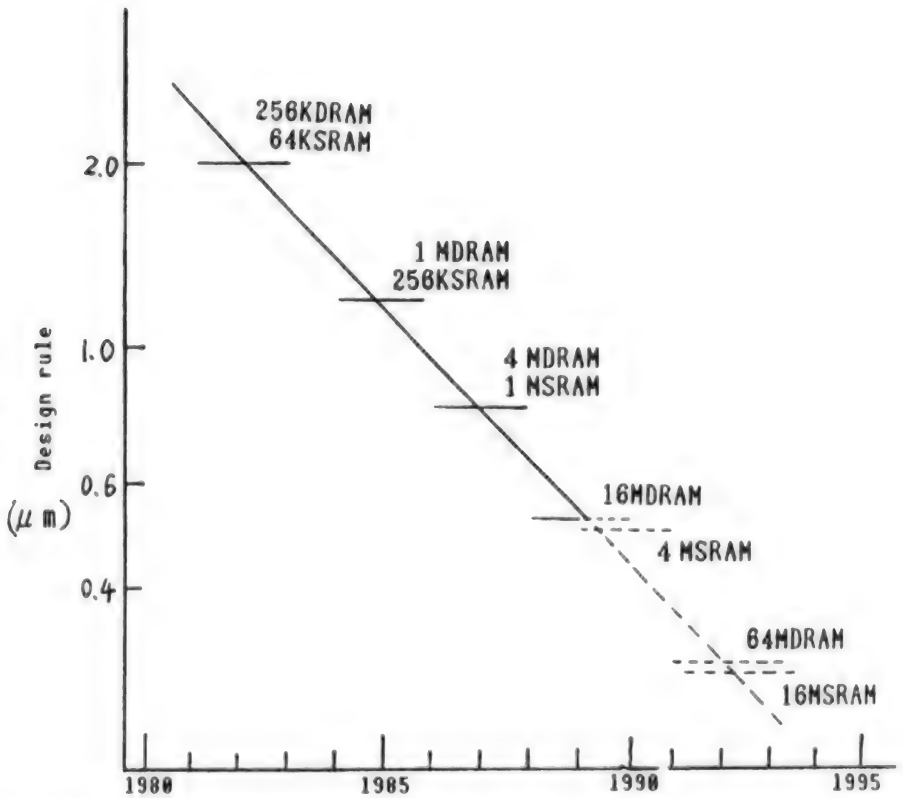


Figure 1. Technological Trend for 1981 and After (ISSCC)
(A fourfold increase in 2 or 3 years)

Device	Cell area (μm^2)	Chip size (mm^2)
4M DRAM	8~10	≈ 80
1M SRAM	≈ 40	
16M DRAM	≈ 4	130~140
4M SRAM	≈ 20	
64M DRAM	1~2	200
16M SRAM	≈ 9	

Note: May depend on a design rule and device structure but the table may cover the entire picture.

Figure 2. Prediction of Chip Sizes

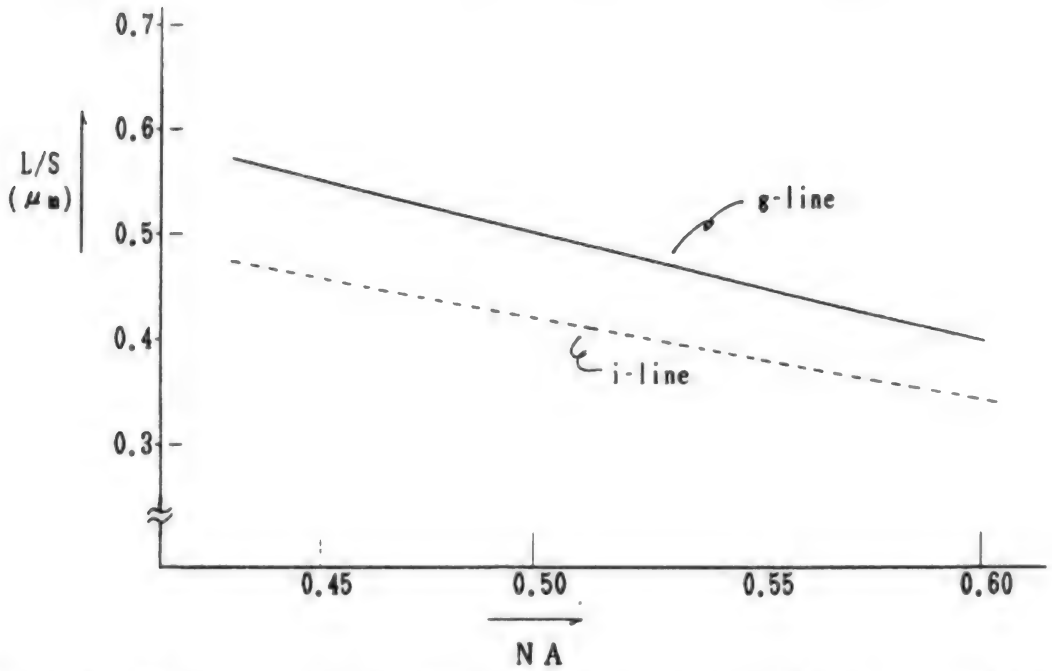


Figure 3. Prediction of Stepper's Resolution Limit (1) <g line, i line>
—0.45 μmL/S is possible with the g line NA 0.55 class
(i line NA 0.45) —

$$Res = k \frac{\lambda}{NA}$$, where k = 0.57 (0.55 μmL/S with g.NA 0.45)

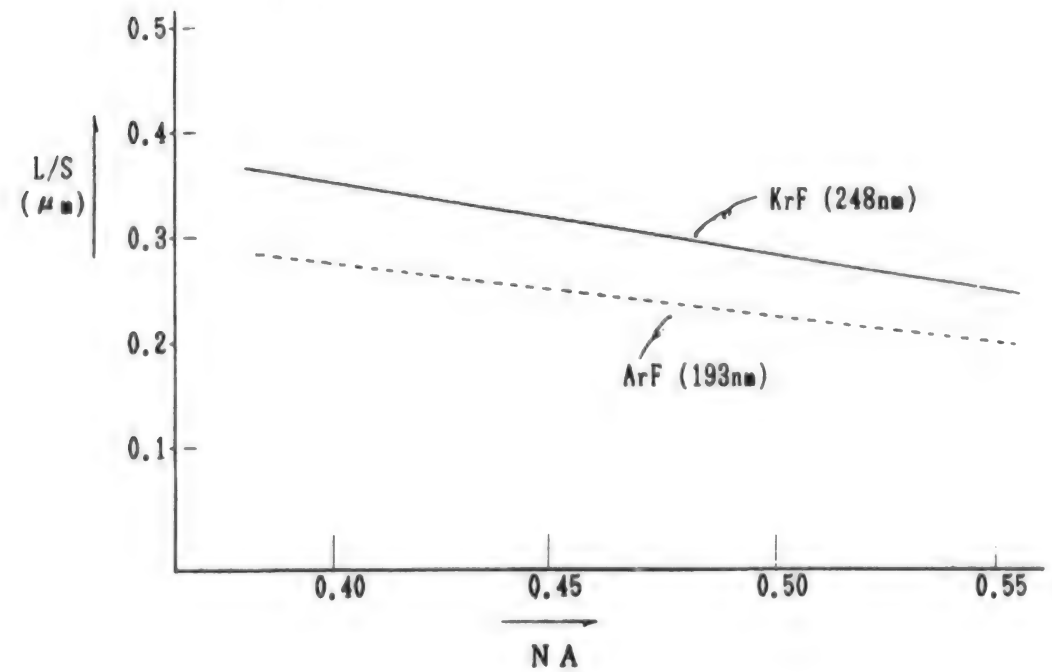


Figure 4. Prediction of Stepper's Resolution (2) <Excimer laser, 248 nm, 193 nm>
—0.28 μmL/S is possible with a KrF laser (248 nm) NA 0.50 —

$$Res = k \frac{\lambda}{NA}$$, where k = 0.57

Device	Design rule	Lithographical technology	Chip size	Starting year for mass production
16M DRAM 4M SRAM	0.6~0.5 μm	g line NA≥0.55 or i line NA≥0.45	130~140 mm^2 (400 mil SOP)	1991-92
64M DRAM 16M SRAM	0.35~0.30 μm	KrF excimer laser (248 nm) NA≥0.45	200 mm^2 (600 mil SOP)	1995-96
256M DRAM 64M SRAM	0.20 μm	SOR (minification?)	260~280 mm^2 (Width: 600 mil SOP)	2000( )

Figure 5. Prediction of Design Rules
From the prediction of chip sizes and stepper resolutions, the forthcoming design rules are predicted as follows:
—— Example of memories = *1 chip memory ——

Maker	Wavelength	NA value	Field size	Marketing year	Remarks
Nikon	g	0.45	15 mm□	1987	
	g	0.54	15 mm□	Dec 1988	
	g	0.45	15 mm□	After 1988	
Canon	g	0.43	15 mm□	1988	
	g	0.45	20 mm□	July 1988	
	g	0.48	15 mm□	June 1988	
Hitachi	i	0.40	15 mm□	1988-	
GCA	i	0.42	15 mm□	Jan 1988	

Figure 6. Development Status of Steppers

1. Stable steppers should be prepared for mass production by 1991

2. For resolution, 0.5 μm should be stably formed.
   g line - NA $\geq$ 0.55
   i line - NA $\geq$ 0.45

3. Field size of 17 mm□ should be possible.

4. Resist process should be completed.

5. Enough throughput should be maintained.

Figure 7. Judgment Reference of Light Exposure Methods--g line or i line (For mass production of 16M DRAM of 4M SRAM devices)

	Good points	Shortcomings
g line	• As it is an extension of conventional technology, its degree of completion is high. • A practical stepper in the NA 0.55 class is foreseeable as of 1988.	• Focus depth becomes shallow and the mass production for over NA 0.55 will be difficult in practice (?).
i line	• Focus depth becomes 20 percent deeper than g line. • Resolution increases by 10 percent for the same focus depth.	• Lens materials are limited. (High permeability, high reflection factor). • Resist process is yet to be completed. • No practical stepper of more than NA 0.45 is foreseen as of 1988.

Figure 8. Comparison Between g Line and i Line

Resist name	Maker name	Resolution (μm)	Sensitivity (mj/cm^2)	Heat resistance (°C)	Remarks
TSMR-V1	Tokyo Applied Chemical	0.55[1]	210	100	Surface hardening type
TSMR-V3	" " "	0.55[1]	210	100	
PFR-Gx100	Nippon Synthetic Rubber	0.55[1]	180	100	
FH-6300	Fuji Hunt	0.55[1]	180	100	
TSMR-365i	Tokyo Applied Chemical	0.50[2]	210	120	Exclusive for i line
R1-7083P	Hitachi Chemical	0.55[3]	170	135	For both g and i line

[1] L/S value with NSR-1505G4D (Nikon NA 0.45)
[2] L/S value with i line NA 0.45.
[3] L/S value with LD-5010i (Hitachi, NA 0.40)

Figure 9. Recent Resist Materials
(Materials for both g line and i line are at almost satisfactory levels in profile.)

Meanwhile, recently developed resist materials have provided nearly satisfactory profiles. It is estimated that these resists will meet the 0.6~0.5 μm rule sufficiently with a forthcoming high NA g line (or i line) stepper.

Concurrently, advanced resist process developments for CEL, REL, etc., have been repeatedly reported. However, although these methods have a considerable effect at the device development stage, in practice there are many control parameters and it may be hard to use them on a practical mass production line.

Further, it is a big task just to maintain junction accuracy. Also, the process side poses a greater problem than the equipment at present and it is necessary to improve resist asymmetry.

3. Present Status and Problems of 0.3 μm Lithographic Technology

As target specifications, a resolution of 0.3 μm L/S and a juncture accuracy of more than $\pm$0.10 μm are required.

The light exposure equipment used for this purpose will not be adequate if a conventional g line or i line is used, but an excimer laser stepper with a shorter wavelength would be satisfactory. Some makers have already marketed prototype steppers.

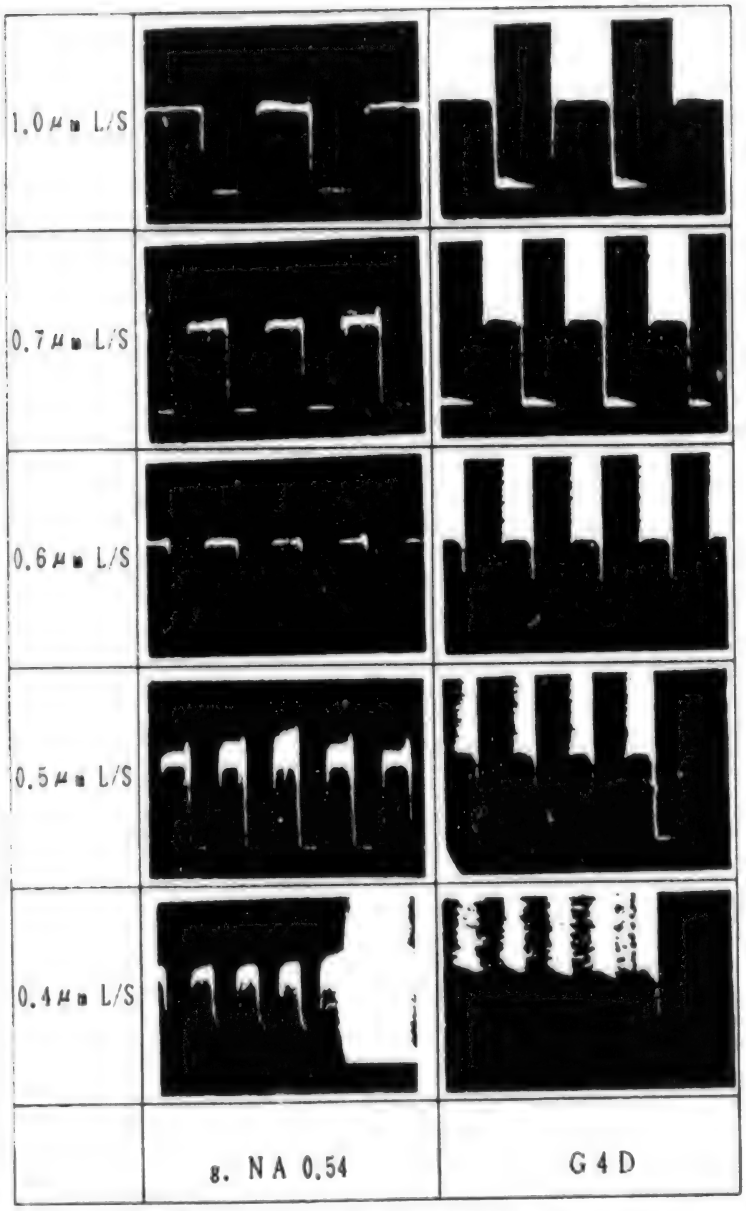


Figure 10. Comparison of Resolutions Between High NA (Nikon g, 0.54) Lens and G4D (Nikon NA 0.45)(1)
Resist: TSMR-V3 1.1 μm thick (Tokyo Applied Chemical)

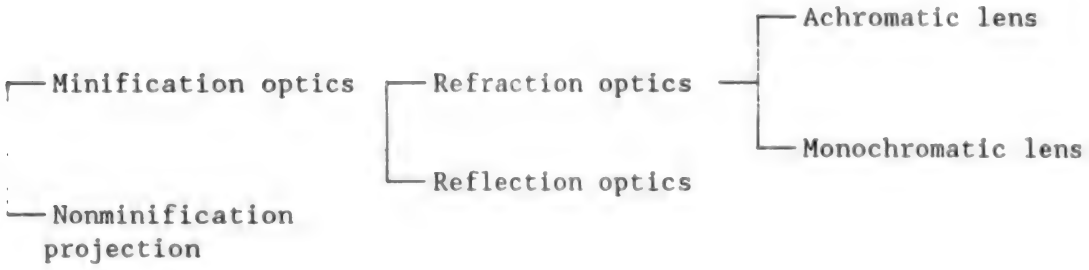


Figure 11. Excimer Laser Projection Optics System
(Minification optics with a monochromatic lens used primarily at present)

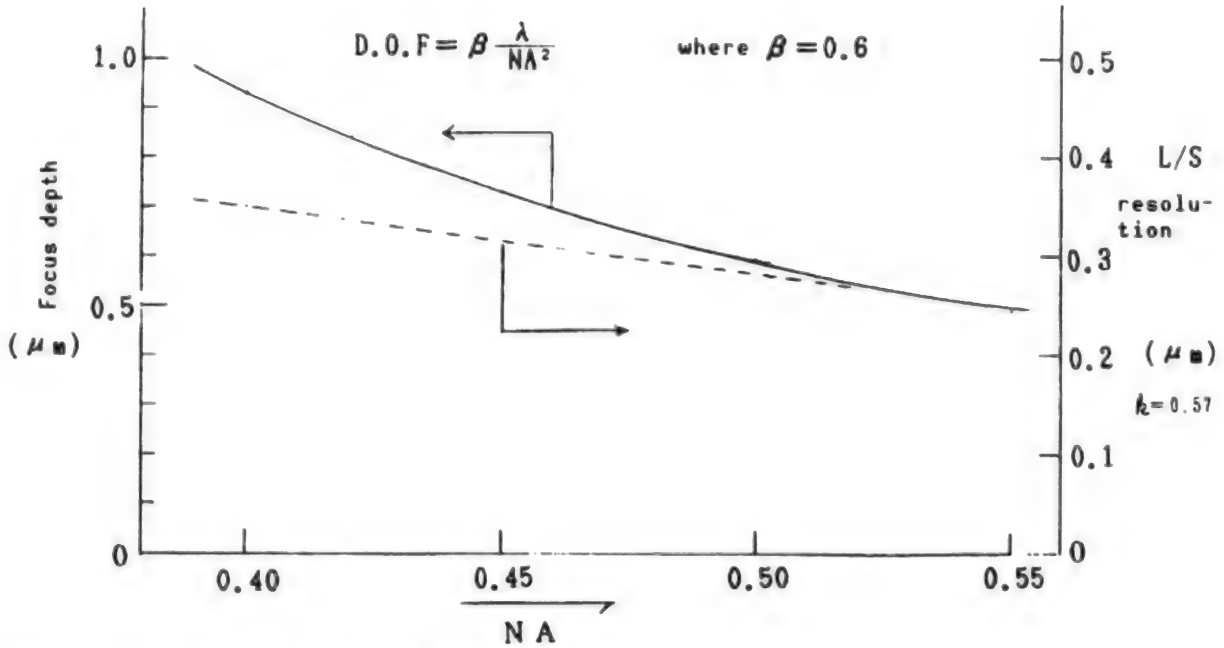


Figure 12. Focus Depth of Excimer Steppers
(Chip leveling is a must for shallowing focus depth)

Maker	Wavelength (nm)	NA	Field size	Year of market release	Remarks
Nikon	248	0.42	15 mm□	April 1988	
Canon	248	≤0.40	15 mm□	June 1988	
GCA	248	0.35	20 mmϕ	October 1987	
	193	0.35	10 mmϕ	1987	Experimental prototype

Figure 13. Development Status of Excimer Steppers
(First generation prototype steppers are almost on the starting line.)

Item	Unit	Target specifications	Present status Wideband laser	Narrowband laser
Wavelength	nm	248	248	248
Spectrum width (FWHM)	nm Wideband laser	0.3~0.4	0.3~0.4	--
	Narrowband laser	<0.003	--	0.003~0.005
Wavelength stability	nm Wideband laser	--	--	--
	Narrowband laser	<0.001	--	±0.001
Mean output	W	>30	>30	1.5~3.0
Pulse energy	mJ	30~100	~100	5~15
Repeat frequency	pps	300~1k	~500	100~250
Gas service life	pulse	$>10^8$	10^6~10^7	10^6~10^7
Window replacement interval	pulse	$>10^8$	10^7~10^8	10^7~^{8}
Service life of electrode, switching elements, etc.	pulse	$>10^9$	10^8~10^9	10^8~10^9

(From Tanimoto, Nikon Co., Ltd., 11th VLSI Forum, March 1988)

Figure 14. Target Specifications and Present Status of Excimer Laser for Steppers

1. Completeness improvement of excimer lasers
   --In terms of stability, long service life, and high repeatability

2. Improvement of alignment accuracy
   --Development of TTL alignment

3. Improvement of focus stability
   --Adoption of chip leveling

4. Toward high NA and high field
   --NA > 0.45 20 mm□

Figure 15. Tasks Facing Excimer Steppers

Resist type	Example of composition	Samples	Problems
Positive			
Polymer decomposition	--	PMMA PMIPK	D.E. resistance Organic solvent phenomenon
Solution speed change type	Cresol novolac + naphtoquinonediazide	MP-2400 PR-1024	Strong light absorption Bad resist shape
Chemical amplification type	Polyphthalaldehyde-onium salt-serylether-onium salt	None	Bad stability Bad linewidth control
Negative			
High polymer bridge type	--	CMS CEL-N	Much swelling (Low resolution)
Alkaline phenomenon bridge type	Cresol novolacbisazide Diazide	RD-2000N	Bad shape (Reverse taper)
Chemical amplification bridge type	Cresol novolac melamine derivative	ECX-1045	Bad stability Bad linewidth control

Figure 16. Diagram of Resist Material System for Excimers

Resist name	Maker	Material name	Capability	Remarks
PR-1024(P)	Toray	Novolac + naftoquinone-diazide	(see text)	Marketed
MP-2400(P)	Shippray	" " "		Marketed
ER-805(N)	Toshiba	Phenol resin + diazo		
STAR-P2(P)	Matsushita	Styrene resin, 3-diazo 2,4-dion derivative		
STAR-N1(N)	Matsushita	Styrene resin, 4,4' diazidediphenyl methane		
Sample positive	Toshiba	Phenol resin		
Sample negative	Hitachi	Polyparahydroquistyren 3,3' diazidephenylsulfone		

Figure 17. Resist Materials for Excimer

	~0.8 μm	~0.5 μm	~0.3 μm
Wafer	No particular limit	LTV or FPD	LTV or FPD
Resist	Evaluation and selection of marketed resist	Development and selection of marketed resist Process development	Resist material development
Quarter development	No particular limit	Temperature and humidity control	Temperature and humidity control
Stepper	Purchase of high NA from usual makers	Selection of g or i Selection of i	Selection of makers Development of stepper evaluation technology
Measurement evaluation	Light Measurement length SEM	IPQC SEM Measurement length SEM	IPQC SEM Measurement length SEM

Figure 18. Features of Future Lithographic Technology

However, the excimer stepper has some intrinsic problems not found in conventional steppers. One is the excimer laser light source itself. There are other big problems, such as wavelength stability, power and service life. Further, a large junction error generated by the off-axis alignment remains to be settled.

From now on, three parties--laser makers, stepper makers, and users--will have to cooperate to ensure progress toward practical applications.

Meanwhile, the focus depth also becomes quite shallow--about ±0.3 μm. It is naturally necessary to improve equipment by such techniques as chip leveling, but it is also necessary to make wafers even flatter and to use multilayer resists.

Resist materials also pose a big problem. Conventional novolac resists do not allow light to permeate to the lower part of the resist due to its strong light absorbing property and it tends to form a triangle shape. Many makers are vigorously developing new resists and it is sometimes necessary to change the conventional resist chemistry as required. It may prove necessary to use multilayer resists to combat shallow focus depth. In any case, the resist process is a key technology for realizing excimer lithography and maximum efforts should be exerted.

4. Future Prospects for Lithographic Technology

After 0.5 μm devices, lithographic technology itself will lead toward enhanced capability devices--that is, lithographic technology will play a more important role than ever. Lithographic technology itself will become a limit technology, including its measurement technology, and even greater demands will be placed on the full range of technological capabilities. Many of these technologies will not be created by a single maker and it is expected that joint development efforts by several makers will become more common.

0.5~0.3 μm Lithographic Technology (2)--EB, X-Ray, FIB--Problems, Prospects for Practical Use

43064001 Tokyo '89 ULSI PROCESS TECHNOLOGY SYMPOSIUM in Japanese 7-8 Dec 88 pp III1-III8

[Article by Tadahiro Takigawa, ULSI Laboratory, Toshiba Corp.]

[Text] **1. Demands for 0.5~0.3 μm Lithographic Technology**

The 0.5 μm 16M DRAM and 0.4~0.3 μm 4M DRAM devices will begin to be marketed around 1990 and 1993, respectively. Development of these devices must begin at least 2~3 years before market release. From this perspective, we must have 0.5 μm and 0.3 μm lithographic technologies by 1988 and 1990. Further, these technologies will require similar systems at the mass production stage in order to shorten the development period. When we think of miniaturization up to a 0.3 μm device, no technologies other than optical lithography are conceivable.

2. EB Lithography

1) Reticle Writing

The main element of optical lithography for some time to come will be a stepper with a minification rate of 5:1. This stepper requires a high-accuracy reticle. To make this reticle, a massive system consisting of an EB resist process, reticle inspection/modification unit, CAD, etc., must be assembled (Figure 1).

Table 1 shows the principal specifications of a recent EB writing unit. This unit, made by Toshiba Machine, is shown in Figures 2-5 as an example of a reticle writing unit.

Along with miniaturization of devices, the beam diameter used for reticle writing must be made smaller. A beam with a diameter approximately one-tenth the pattern size is required, as the writing speed slows at a rate inversely proportional to its square. Table 2 shows the beam diameters and writing times required for reticle writing of 4~64M devices. After the 64M devices, a high-capacity new generation EB unit will be required for reticle writing. For the generation change to the EB unit, the entire system covering the EB resist process, reticle inspection/modification unit, CAD,

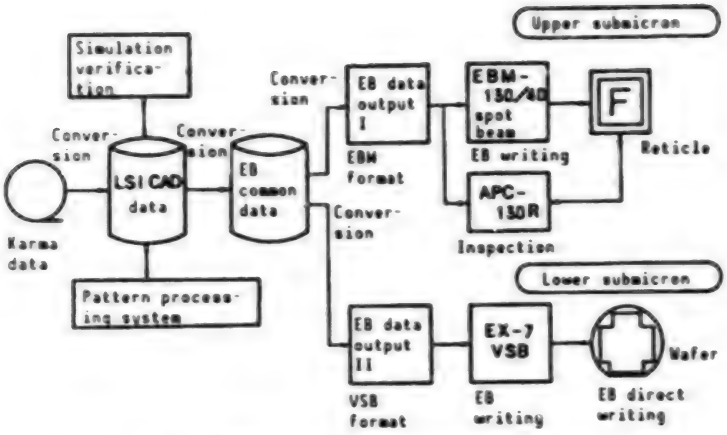


Figure 1. Submicron EB Lithography System

Table 1. Principal Capabilities of EB Writing Unit

Developer (maker)	Perkin-Elmer	Toshiba Machine	Hitachi	Perkin-Elmer	Telecommunications Lab.	Toshiba	Bell Laboratories
Unit name	MEBES-II	EBM-160/80	HL-600	AEBLE-150	EB-60	EX-7	EBES4
Main objective	Mask/reticle	Mask reticle	Direct writing	Direct writing	Direct writing	Direct writing	Mask/direct writing
Beam formation	Spot	Spot	Variable rectification	Variable rectification	Variable rectification	Variable rectification	Spot
Beam diameter	0.1~1 μmφ	0.1~1.2 μmφ	Max 6 μm□	Max 1.5 μm□	—	Max 1.6 μm□	1/2, 1/16 μmφ
Deflection system	Raster	Raster	Vector	Vector	Vector	Vector	Vector
Number of deflection stages	1	1	2	2	2	2	3
Stage stepping system	Continuous stage movement	Continuous stage movement	S & R	Continuous stage movement	Continuous stage movement	Continuous stage movement	Continuous stage movement
Accelerated voltage	20 kV	20 kV	30 kV	20 kV	30/15 kV	50 kV	20 kV
Current density	~60 A/cm²	~60 A/cm²	5 A/cm²	75 A/cm²	70 A/cm²	200 A/cm²	1600 A/cm²
Address size	Min. 0.05 μm	Min. 0.1 μm	0.025 μm	0.0156 μm	0.02 μm	0.01 μm	Min. 1/16 μm
Minimum writing size	0.2 μm	0.4 μm	0.5 μm	0.5 μm	0.5 μm	0.25 μm	0.25 μm
Deflection field	0.512 mm	0.256 mm	3 mm□	2 m□	2.6 mm□	0.5 mm□	0.28 mm□
Alignment accuracy	±0.12	±0.12	±0.15 mm	±0.15 mm	±0.1 μm	±0.1 μm	—
Throughput	1 chip/time (0.25 μm mode)	1 chip/time (0.25 μm mode)	Up to 3 chips/time 4-inch wafer	4-29 chips/time 4-inch wafer	28 chips/time 4-inch wafer	5 chips/time 4-inch wafer	2 chips/time (1/8 μm mode)

Table 2. Relationship Between Pattern Size, Size Increase, and EB Writing Unit Throughput

Device (pattern size)	Minimum pattern size of 5-times reticle (X)	Size increase (ΔX)	Throughput of EBM-130/40	Throughput of EBM-160/80
4MDRAM (1 μm)	5 μm	0.5 μm	1.3 chips/hr	2.6 chips/hr
4MDRAM (0.8 μm)	4 μm	0.5 μm or 0.25 μm	1.3 chips/hr 0.3 chips/hr	2.6 chips/hr 0.6 chips/hr
16MDRAM (0.5 μm)	2.5 μm	0.25 μm	0.3 chips/hr	0.6 chips/hr
64MDRAM (0.3 μm)	1.5 μm	0.1 μm	0.05 chips/hr	0.1 chips/hr

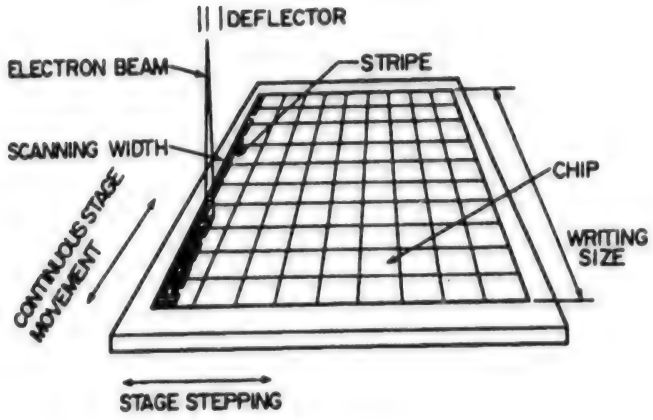


Figure 2.

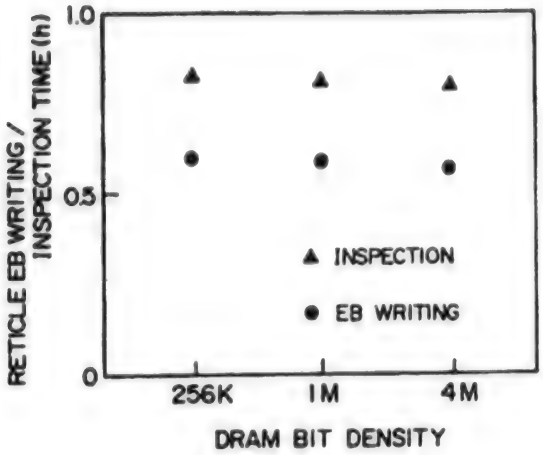


Figure 3.

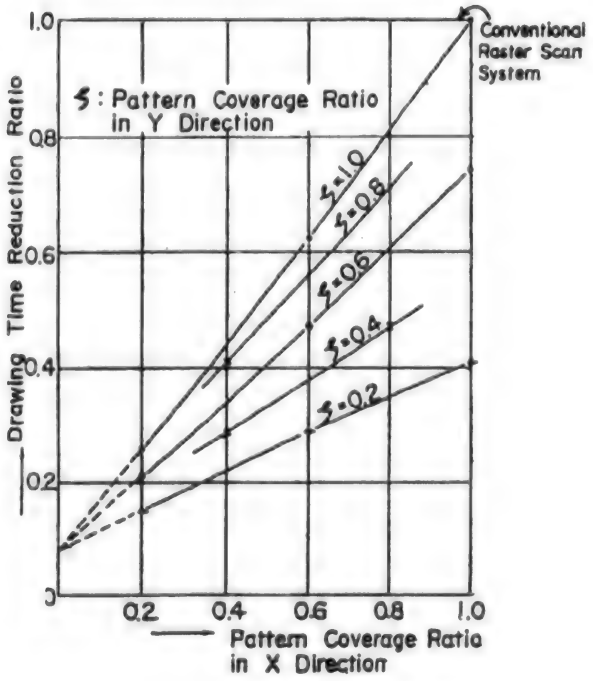


Figure 4.

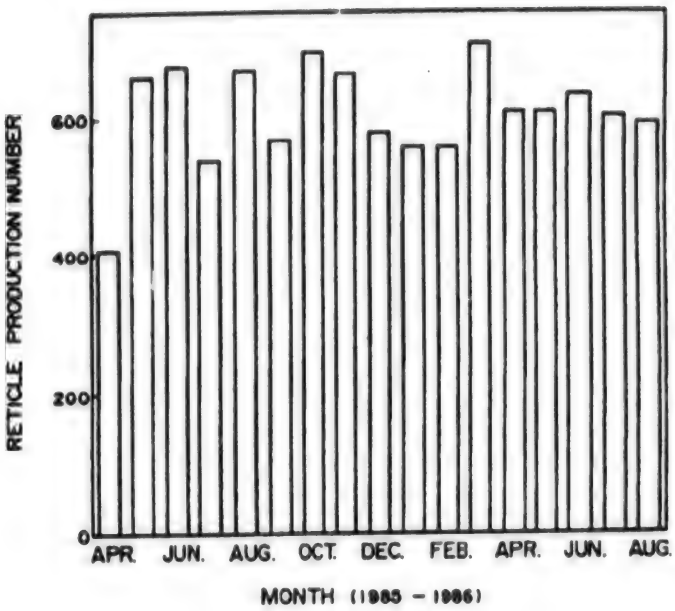


Figure 5.

etc., must be changed. From now on, makers will develop a new generation reticle manufacturing system with each other.

2) Direct Writing Technology

The device miniaturization rate is faster than the optical lithographical resolution improvement rate and the requirements for a 0.6 μm device still cannot be readily met.

Further, to develop 0.5 μm devices it is necessary to study the characteristics of devices up to about 0.3 μm. Its unique pattern formation means EB direct writing. The test pattern scale used for developing DRAM devices is as big as the device itself. Therefore, it is important that the EB unit for that wiring must be connected to CAD. For example, Toshiba's direct drawing unit EX-7 is introduced in Figures 6-11 and Table 3. Because the accelerating voltage is as high as 50 kV, it is possible to write LSI patterns of 0.25 μm. Such units will be increasingly important for developing future devices.

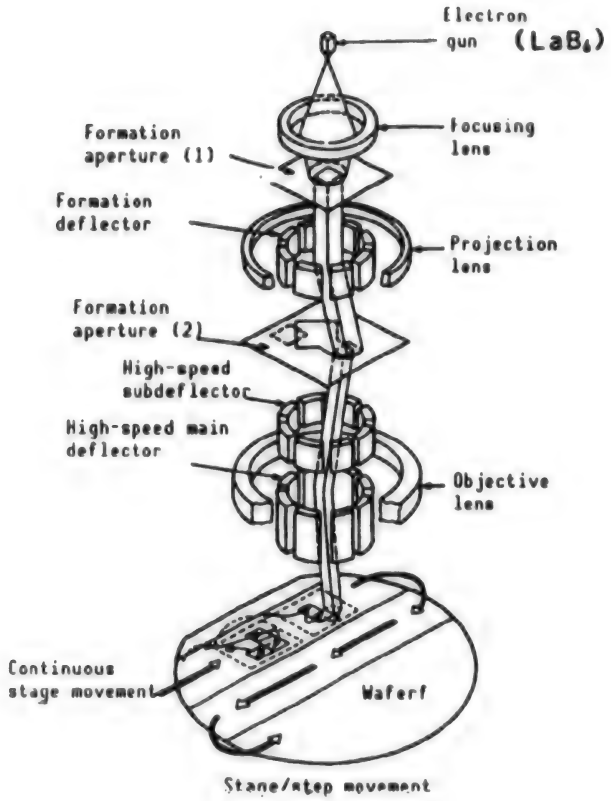


Figure 6. Simulation of EX-7 Writing System

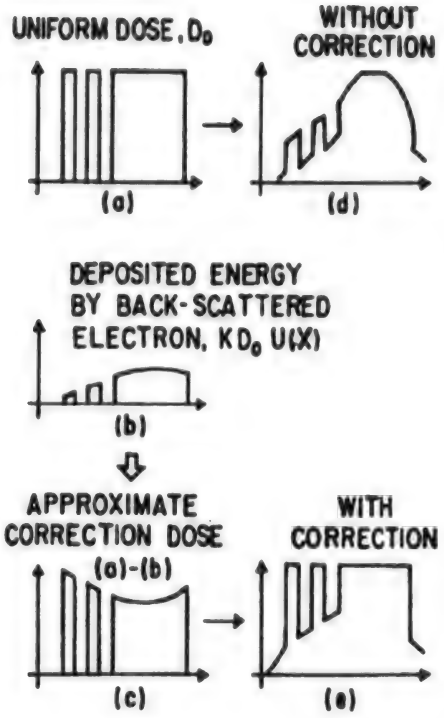


Figure 7.

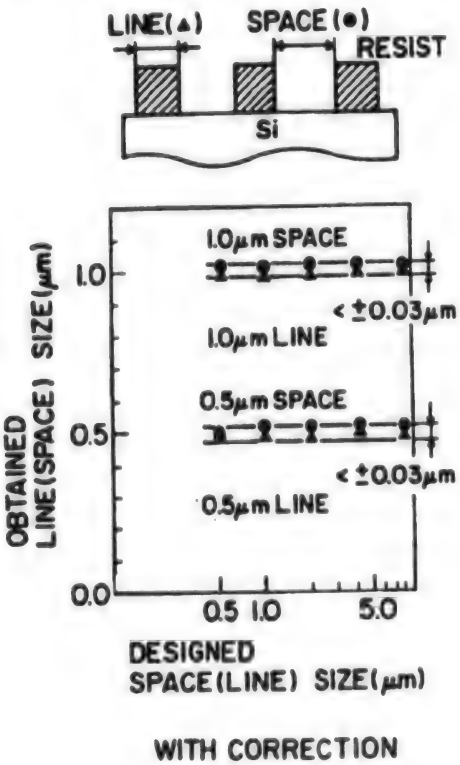


Figure 8.

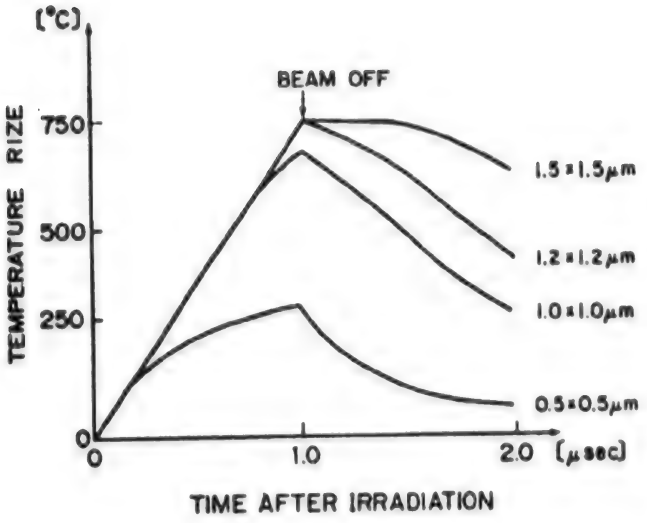


Figure 9.

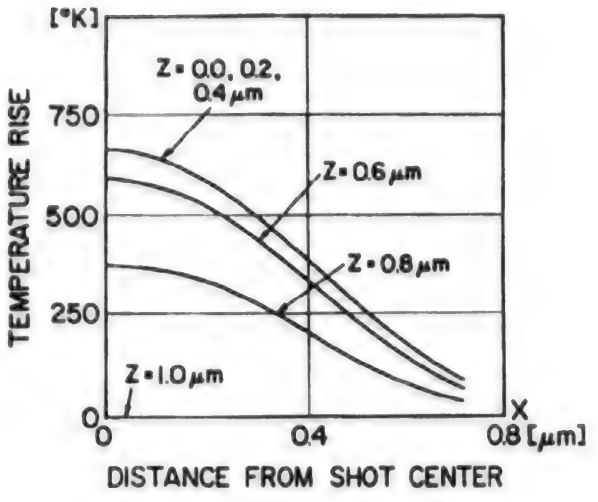


Figure 10.

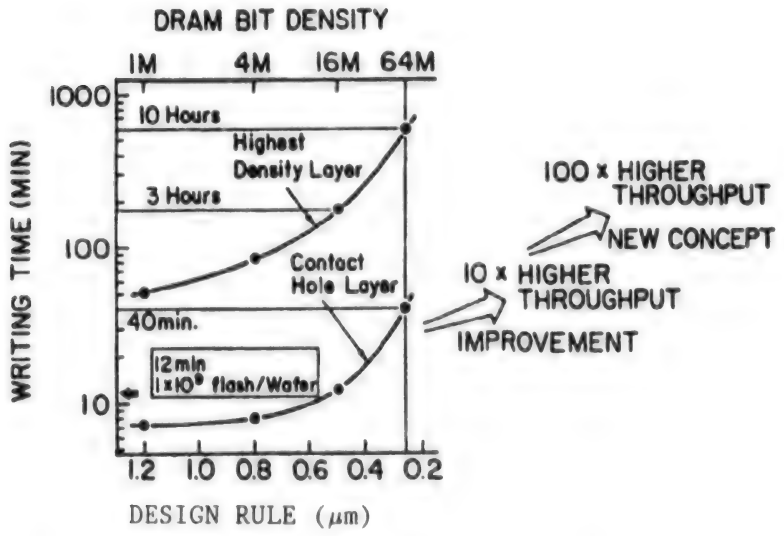


Figure 11. Writing Time for 5-Inch Wafer

3. X-Ray Lithography

X-ray lithography has a deep focus depth and allows a comparatively large field size. For processes such as aluminum wiring formation, some requirements for its use are heard even now, if X-ray lithography is possible, but it may take a little time before it can be put to such practical uses as some problems remain to be solved.

Figure 12 shows the development tasks for X-ray lithography. The principal development tasks are X-ray mask, SOR facility, vertical stepper, and resist. Table 4 shows the present status and targets of X-ray lithography development.

Table 3. Example of Application for Massive Patterns (Using 14 MIPS machines)

	Test device (test circuit 1stAl▪:0.5 μm	Gate array personalized ▪ 2.0 μm	4M DRAM (element separation layer 1/2 minification version) 0.5 μm	
Size	7.5 mm x 15 mm	10 mm x 10 mm	4 x 9 mm	
Resist	Positive	Negative	Positive	Negative
Preprocessing (data conversion)	0.312 hour	0.121 hour	0.092 hour	0.087 hour
Correction processing	0.777 hour	0.359 hour	0.455 hour	0.345 hour
Post-processing (shot division and data compression)	0.228 hour	0.220 hour	0.166 hour	0.150 hour
Total	1.317 hour	0.923 hour	0.758 hour	0.595 hour

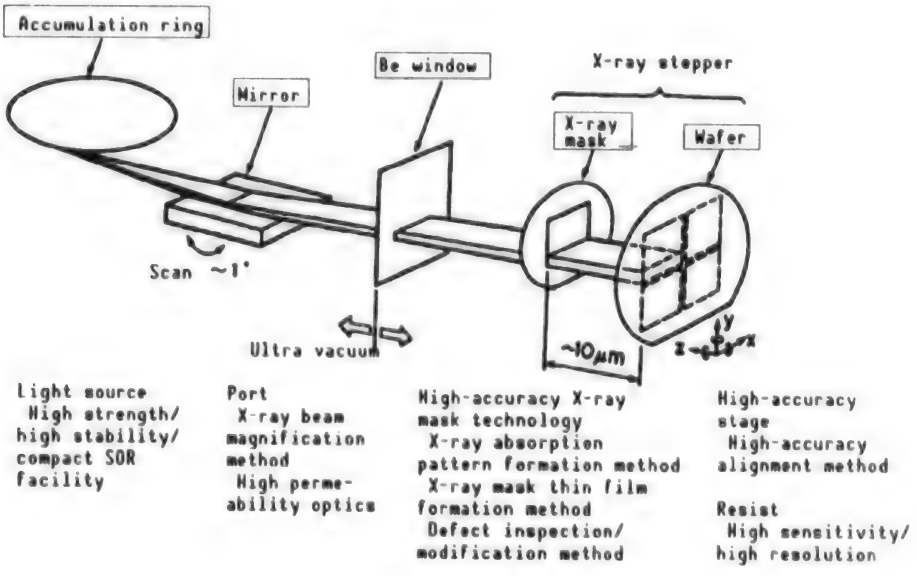


Figure 12. Radiation Light X-Ray Exposure Outline and Main Development Tasks

Table 4. X-Ray Lithography Target and Present State

	Target	Present state
Device	256M DRAM	Ring oscillator
Minimum feature size	<0.25 μm	0.25~0.5 μm
Throughput	40/h•8-inch wafer	5~10/h•4-inch wafer
Resist sensitivity	100 mJ/cm^2	1,000 mJ/cm^2
Mask		
Overlay accuracy	<±0.005 μm	~0.2 μm
EB writing accuracy	~±0.03 μm	~±0.15 μm
Measuring accuracy	~+0.01 μm/25 mm	~0.1 μm/100 mm
Inspection	~0.06 μm	~1 μm
Repair	~0.06 μm	~1 μm

The primary feature of X-ray lithography is nonmagnification proximity light exposure. For that reason, an ultrahigh accurate mask is required. To realize this, the X-ray mask itself--such as an X-ray mask membrane--an X-ray absorption body's stress accuracy control (Figures 13-15) and its peripheral technologies, such as an EB writing unit for the X-ray mask, a defect inspection unit, a size measurement unit, a defect modification unit, etc.--must be developed. There is no need to say that it is necessary to improve stepper accuracy. Figures 16-20 introduce vertical steppers for SOR light. Further, to realize a high throughput in X-ray lithography, it is necessary to increase the permeability rate of the X-ray window sufficiently and to intensify the SOR light strength. To achieve X-ray lithography, the technologies described above must be developed in parallel. These technologies are being vigorously pursued primarily by the West German Franhoffer Laboratory, IBM in the United States, and NTT and Soltech in Japan. Some results have been announced. These and other institutions will pave the way into the 21st century for X-ray lithography development.

4. FIB Technology

Figure 21 shows an example of an FIB unit. Figure 22 shows an example of its application. This kind of unit has been increasingly used since 1987. This is due to the recognition that it is necessary for analyzing defective LSIs. It is expected that their use will continue to grow.

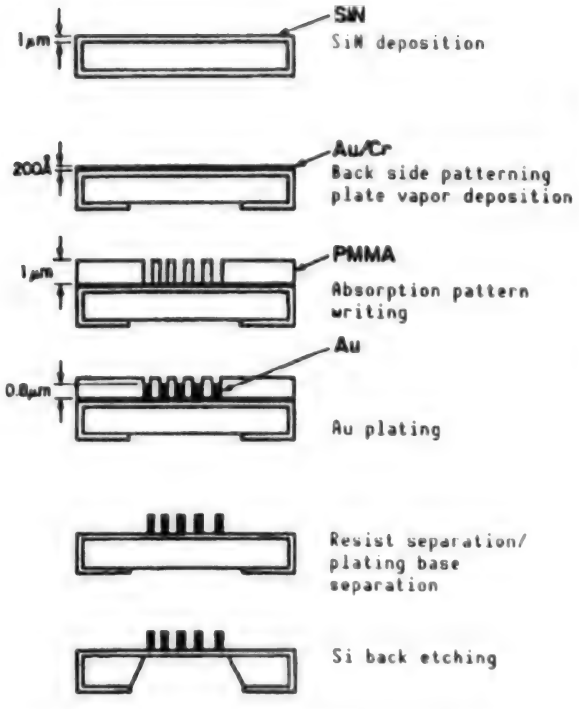


Figure 13. Mask Manufacturing Process

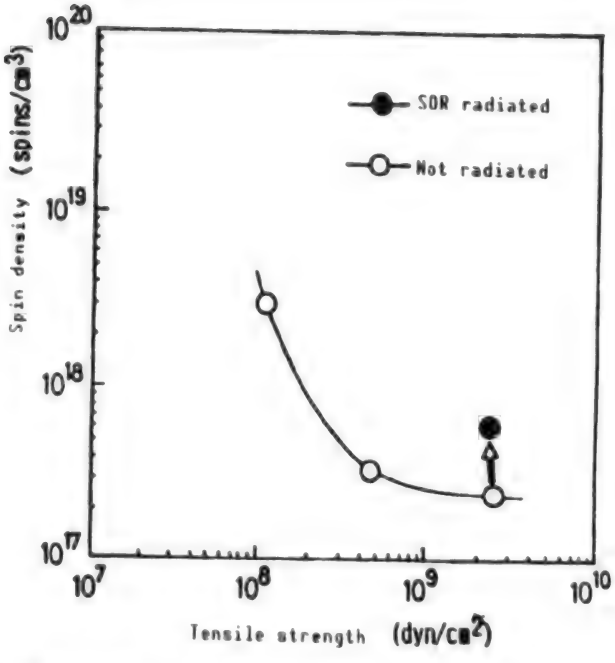


Figure 14. Spin Density of SiN_x Film

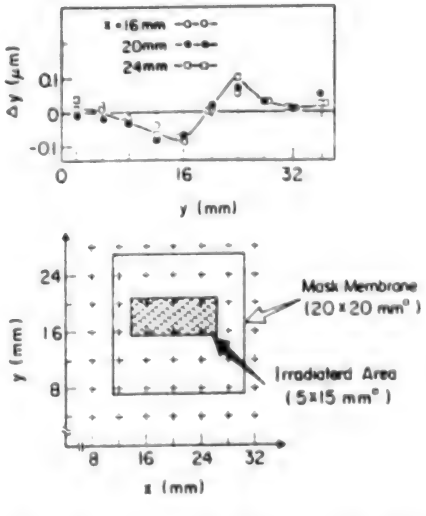


Figure 15. Pattern Displacement Configuration for a SiN Film

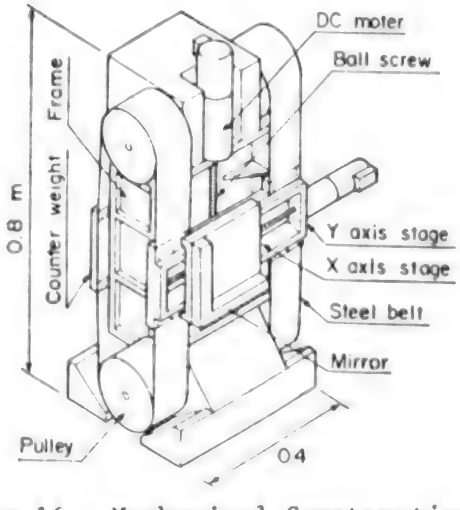


Figure 16. Mechanical Construction

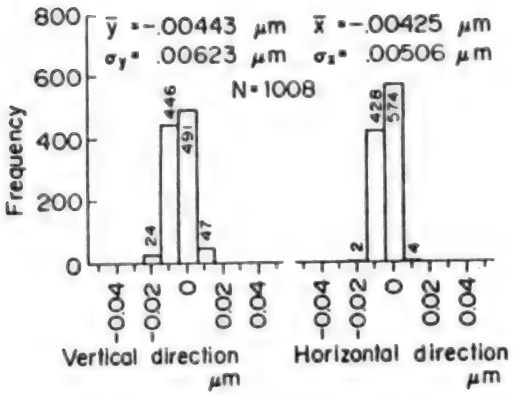


Figure 17. Positioning Error Distribution N = 1008

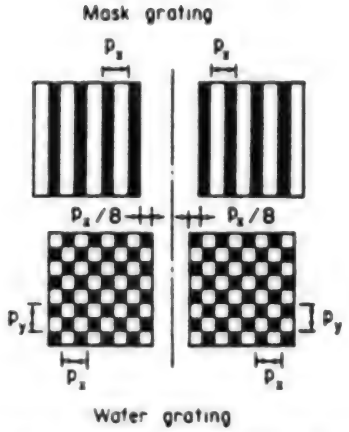


Figure 18. Spatially Phase Shifted Mask and Wafer Gratings

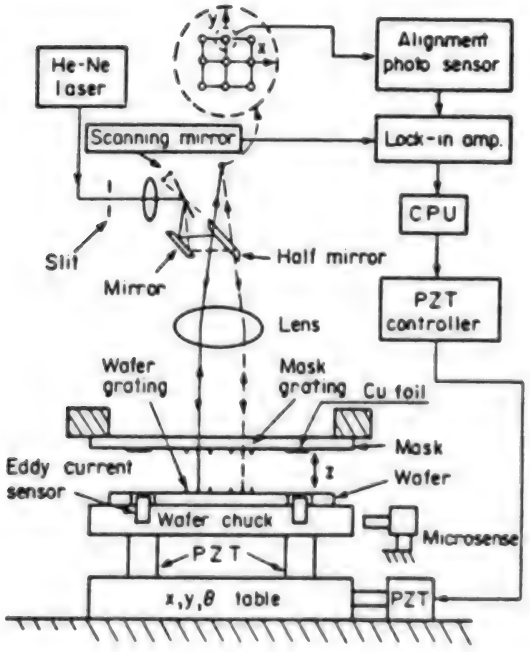
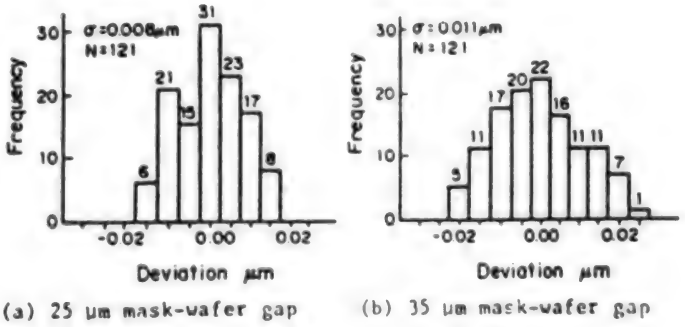


Figure 19. Experimental Alignment Apparatus



(a) 25 μm mask-wafer gap (b) 35 μm mask-wafer gap

Figure 20. Repeatability Measurements for Detection and Positioning Accuracy

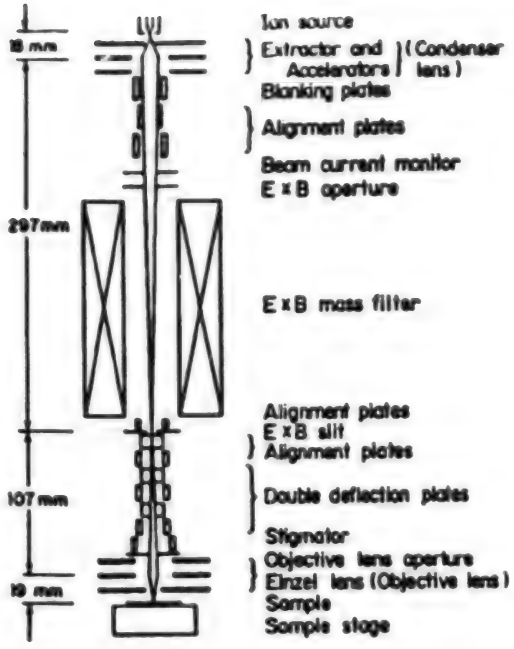


Figure 21.

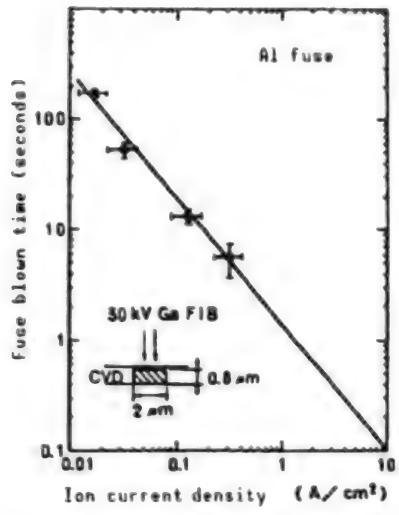


Figure 22. Ion Current Density Dependance While Fuse Is Blown

5. Conclusion

The EB writing unit for reticle writing is a must for the manufacture of 0.5~0.3 μm LSIs. Also, along with the coming resolution limit of optical steppers, EB direct writing units will become necessary for further LSI technological development. X-ray lithography will be used after the 0.3 μm device age as its development scale is massive and it requires a lengthy development period. FIB technology is being accepted by LSI design engineers for analyzing defective LSI devices, and its growth is assured.

0.5~0.3 μm Etching Technology--Problems, Solutions

43064001 Tokyo '89 ULSI PROCESS TECHNOLOGY SYMPOSIUM in Japanese 7-8 Dec 88 pp IV1-IV6

[Article by Nirotoshi Arikado, ULSI Laboratory, Toshiba Corp.]

[Text] **1. Introduction**

Reactive ion etching (RIE) has been widely used as a miniaturization technology since it was introduced for 3 μm devices, starting from the 64K DRAM, which was dubbed the first stage of ULSI. Even though this technology has problems because of radiation damage, it is expected that it will continue to be used. This article briefly describes the problems and possible countermeasures in developing 0.3~0.5 μm devices.

2. Various Demands for Etching Technology

The problems that are expected to appear in the course of developing 0.3~0.5 μm devices can be summarized as follows:

(i) Fabrication of high aspect ratio

To form miniaturized patterns, a multilayer resist process, such as the three-layer resist method, will be used on a full-scale basis. Further, even when the pattern size becomes smaller, the Al wiring, insulation film, etc., will not be thinner and the aspect ratio in etching will be increased to 3~4. In RIE, ions incidental to the wafer exist after hitting neutral particles and are bent in that direction. Therefore, it is difficult to etch a high aspect ratio pattern uniformly. Depending on cell structure, etching can present a complex processing problem, such as how to etch shallow and deep contact holes simultaneously.

(ii) High selection ratio

The thickness of gate oxidized film will be less than 100 A. Further, the diffusion layer depth will be around 0.1 μm. For these reasons, in etching gate electrodes and oxidized films, a very high selection ratio will be required.

(iii) Fabrication accuracy

The allowable pattern conversion difference will be a little less than 10 percent of pattern size depending on processing. In RIE, even if etched vertically, a retreat of the resist end and a pattern conversion difference due to a side wall protection film occur in practice. In conventional devices, these problems were almost negligible. In 0.3~0.5 μm devices, however, they pose real problems. In particular, a minimal size variation around the gate electrode leads to a threshold voltage change in the transistors.

(iv) Etching of new materials

Conventional LSIs were mainly composed of Si,Si compounds and Al. However, new materials of high derivatives such as W and Mo, together with various metal silicides and Ta_2O_5, are now being used to improve element characteristics. Depending on the materials used, no high vapor pressure compounds are used as these would make etching very difficult.

(v) Radiation damage

Radiation damage has been a problem ever since RIE was introduced. For example, in contact hole etching, impurities introduced into the diffusion layer and a layer with a diffused crystal grid can be removed in post processing, but with 0.3~0.5 μm devices, these are hard to remove as the diffusion layer is shallow.

3. Recent New Technologies

In order to etch high-aspect patterns evenly, the etching pressure must be lowered and the ion direction oriented uniformly. A magnetron and ECR are possibilities. Low temperature etching, which has recently attracted attention, lowers the reaction probability between the radical and substrate, and suppresses the undercut. Selectivity in etching depends either on (i) the intrinsic reaction difference for the materials, or (ii) on a selective accumulation (for example, SiO_2 RIE) of thin films on the surface of under materials. In RIE, the etching materials and under materials are either decomposed or activated by the ion impact, making the intrinsic reaction difference negligible. Therefore, in RIE, the selectivity ratio is generally smaller than that of the plasma etching. Recently, it was reported that a high selectivity ratio was attained by cooling the substrate and selectively condensing the etchings into under materials.

Further, the down-flow system, which uses the radical only, has attracted attention as a high selectivity ratio process that produces no damage at all. This is accomplished through such techniques as a highly selective separation of nitride films and high-speed separation of resists.

4. Conclusion

The above provides a brief description of some problems and possible solutions for etching technology in the forthcoming 0.3~0.5 manufacture device age. RIE has sufficient capability as far as fabrication is concerned. moving toward processes that require less energy may be an answer in view of the selectivity and radiation damage to the under-materials, but orientation becomes worse at lower energy levels. It is necessary to break through this tradeoff.

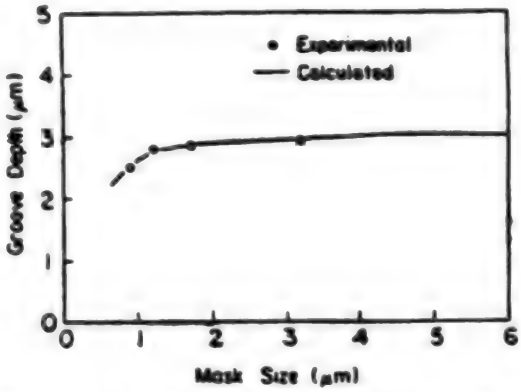


Figure 1. Pattern Dependency of RIE Unit

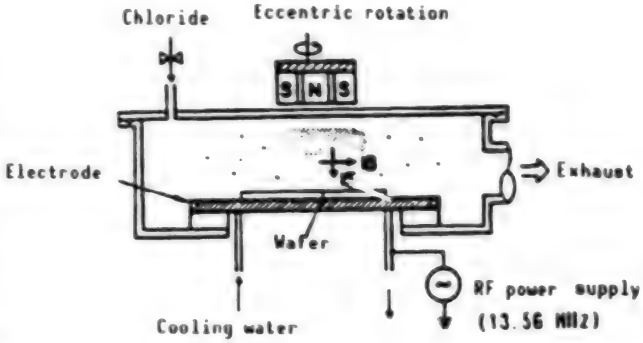


Figure 2. Magnetron RIE Unit

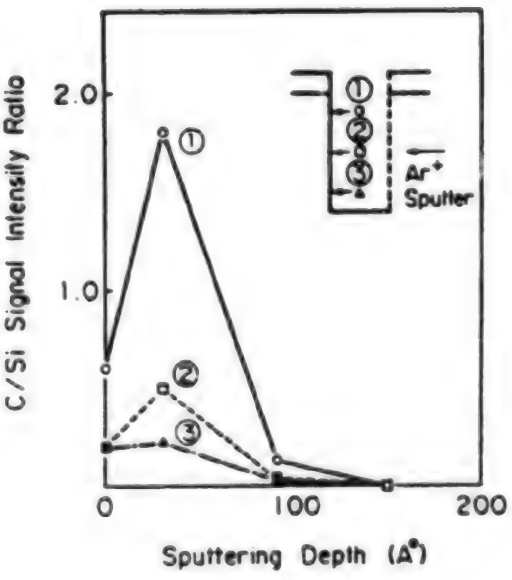


Figure 3. Damage to the Side Wall

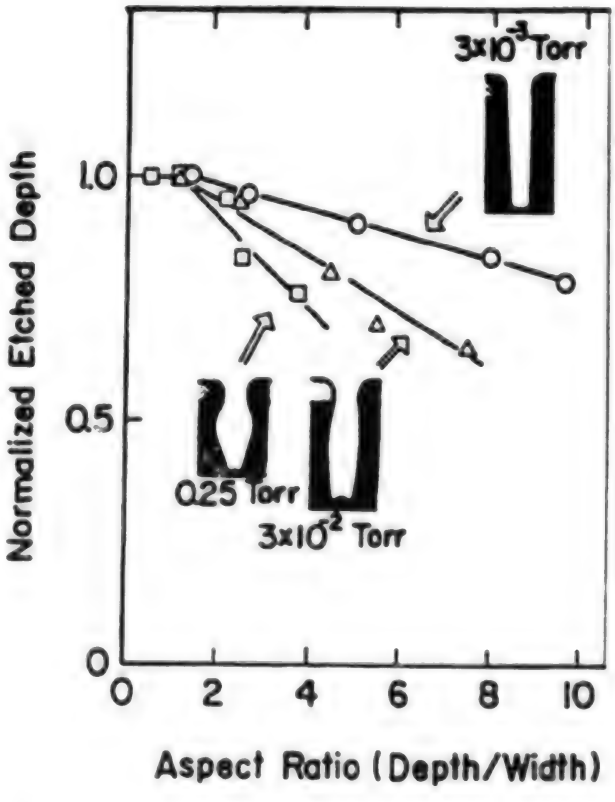


Figure 4. Pattern Dependency

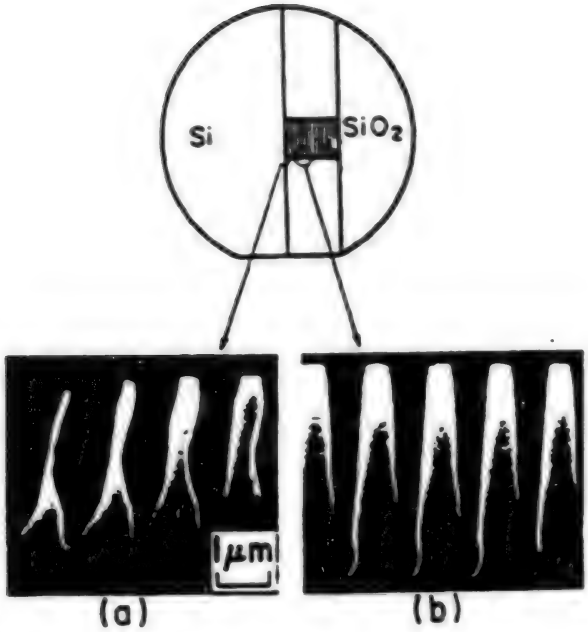


Figure 5. Ion Bending Due to Chargeup

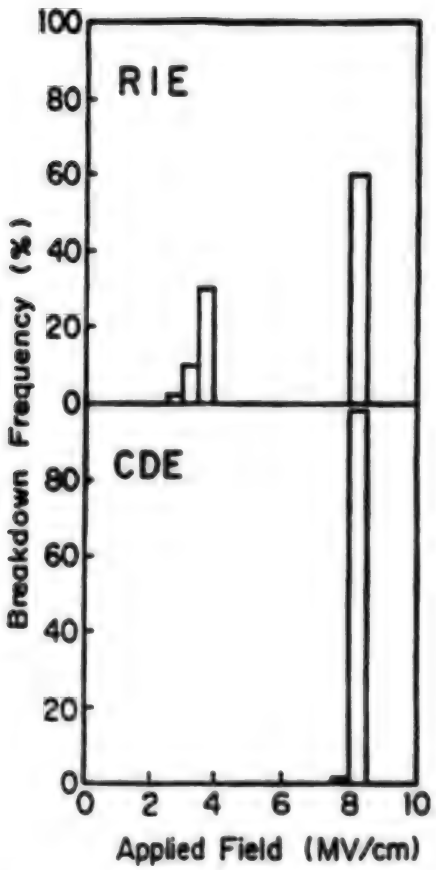


Figure 6. Gate Breakdown

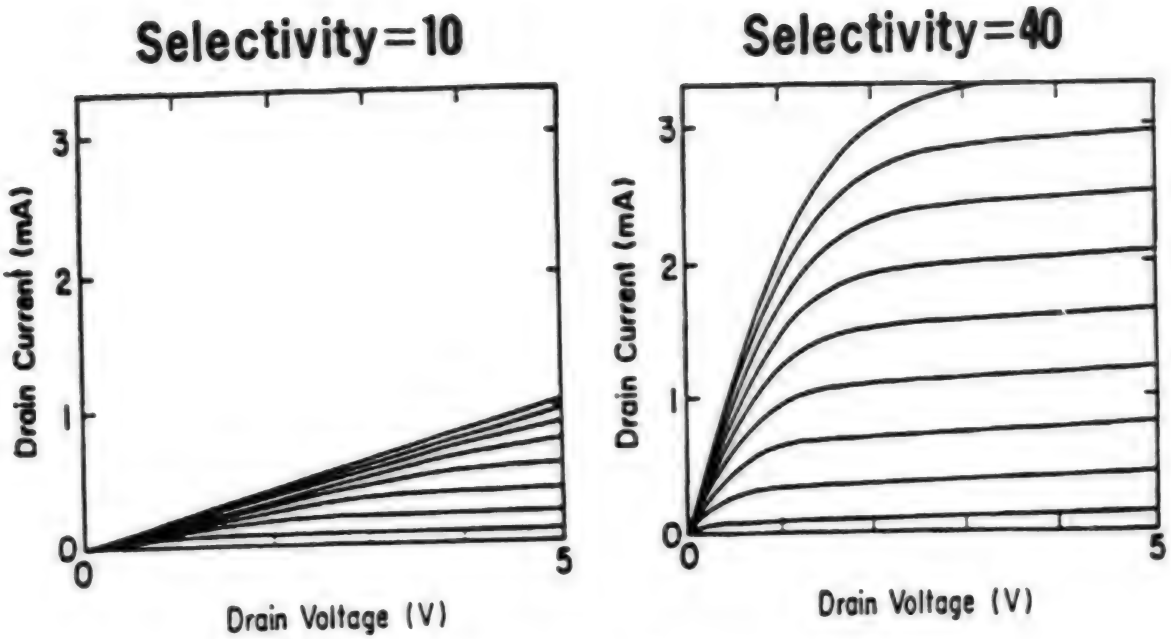


Figure 7. Transistor Characteristics

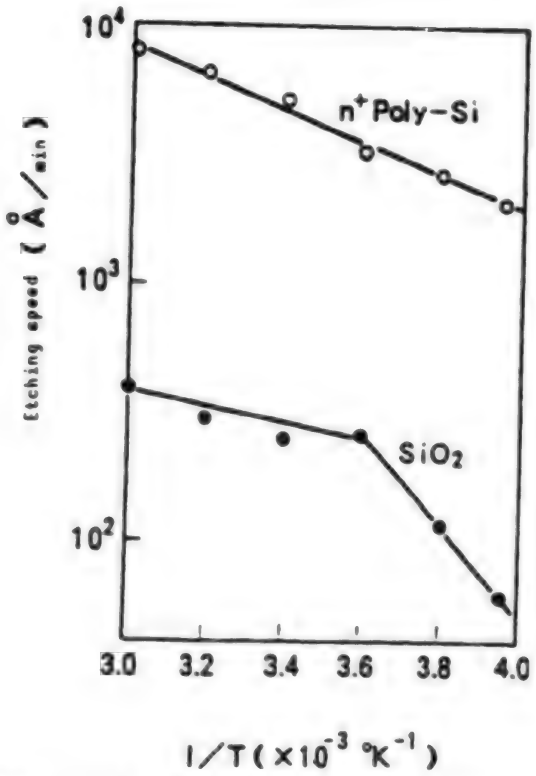


Figure 8. Relationship Between Etching Speed and Temperature

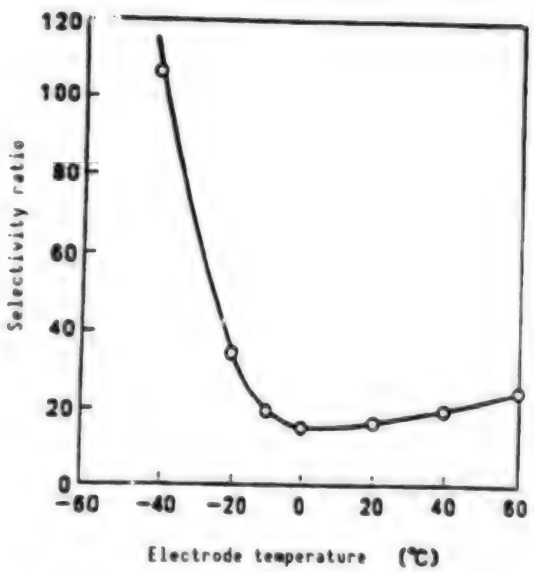


Figure 9. Temperature Change of Selectivity Ratio

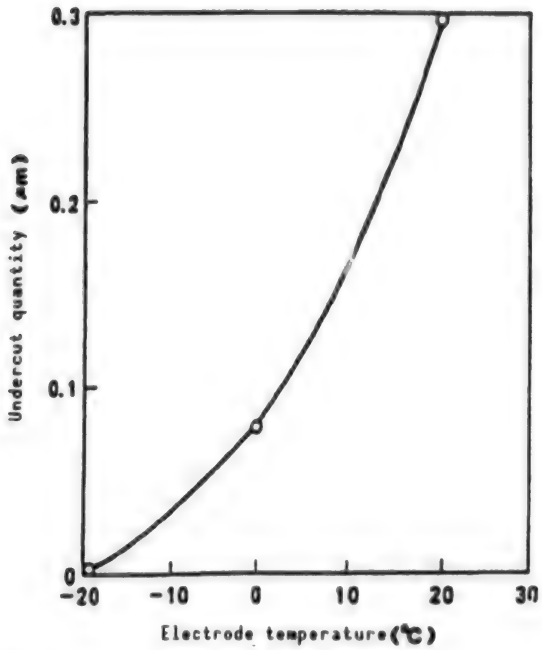


Figure 10. Undercut Temperature Change

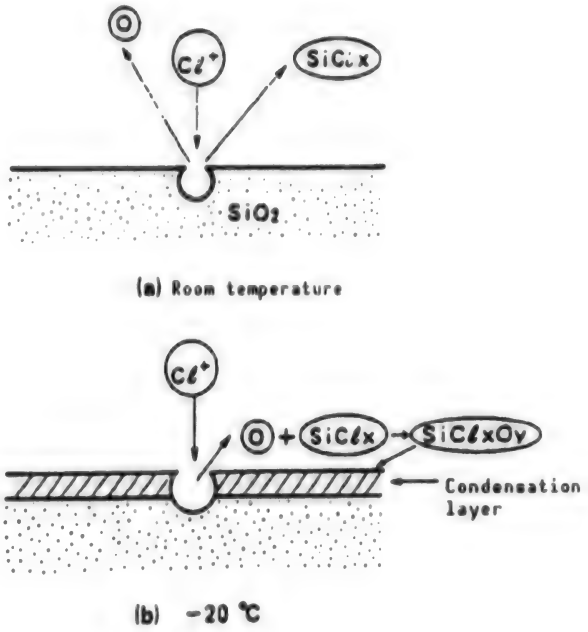


Figure 11. Reaction Model

0.5~0.3 μm CVD Technology--Tasks, Prospects--Centering on Process Technology

43064001 Tokyo '89 ULSI PROCESS TECHNOLOGY SYMPOSIUM in Japanese 7-8 Dec 88 pp V1-V7

[Article by Mitsuru Sakamoto, ULSI Development Headquarters, NEC Corp.]

[Text] **1. Foreword**

CVD technology is diversified and extensive in its methods and applications. Si devices, which sparked the drive toward device miniaturization, and in particular the DRAM manufacturing process, are used effectively for insulation films, semiconductor films, and metal film formations as shown in Table 1. This article describes only the CVD technology for insulation films (derivative films) necessary for ULSIs from 16M to 64M DRAM devices.

Table 1. Application of CVD Technology (Related to Si)

CVD film	Insulation film	SiO_2, doped SiO_2(PSG,BPSG, BSG,AsSG) Si_3N_4, SiON, Al_2O_3, H_fO_2
	Semiconductor film	Single crystal Si, multicrystal Si, amorphous Si, microcrystal Si, SiC
	Metallic film	W, Al, Ti, Ta, Mo, silicide
	Metallic compound	TiN, WN, etc.

2. Applications of Insulation Film CVD Technology

The CVD insulation films used in ULSIs (the number of elements = 10^7~10^9 per chip) starting from the 0.6~0.5 μm design rule are shown in Table 2.

So far, the development of an insulation film CVD has been, rather than creating a new film, mainly in the direction of improving conventional films by enhancing uniformity, reducing particle generation, improving cladding, lowering the accumulation temperature, realizing a higher throughput, etc. However, from now on, among the applications shown in Table 2, there will be increasingly greater demands for the following:

Table 2. Application for CVD Insulation Film

	Application	Film type	Demands for filming
Insulation film	Trench isolation	SiO_2, doped SiO_2, SiON	High embedding, low stress, HF resistance, high purity
	Diffusion source	BsG, AsSG SbSG, PSG	High cladding, high purity
	Gate film	SiO_2, SiON, Si_3N_4	High quality, thinner film
	Capacitance film	SiO_2, Si_3N_4 high derivative film	High quality, thinner film, high ϵ
	Side wall film	SiO_2, Si_3N_4	High cladding, high quality
	Interlayer insulation film I	PSG, BPSG AsSG	Low temperature reflow, high cladding
	Interlayer insulation film II	SiO_2, PSG (SOG)	High flatness, stress control, low damage, low ϵ
	Passivation film	Si_3N_4, SiON SiO_2	Humidity resistance, NA resistance, low damage

(1) New insulation film formation (high derivative rate film, low derivative rate film)

(2) Embedding and planarization

(3) Cleanliness

(4) Stress control

(5) Low damage

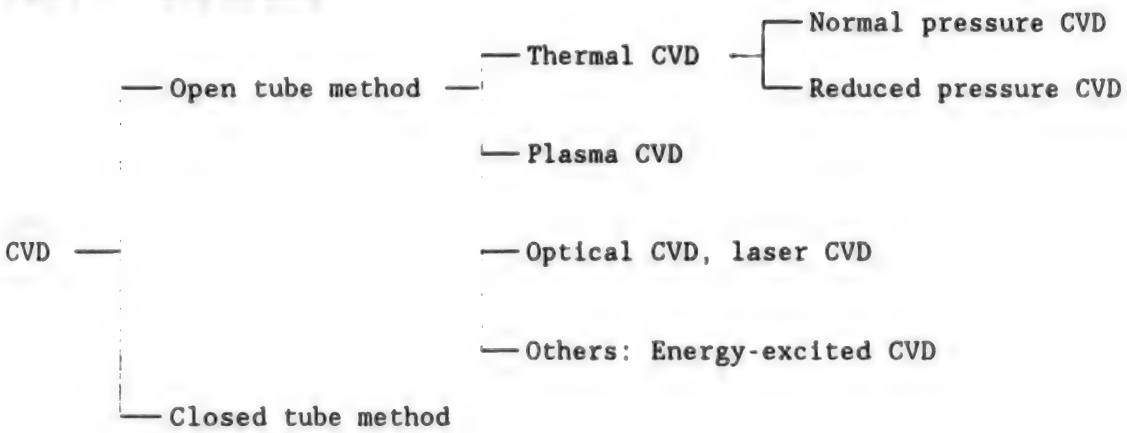
(6) Larger diameters (8 inch ϕ)

3. Present State of Various CVD Methods

Various CVD methods are possible based on the basic CVD principle as shown in Table 3. From these methods, the CVD unit system will be expected to have the following growth factors:

(1) Shape and structure of the reaction chamber
(2) Relationship between the reaction gas flow and the substrate
(3) Substrate temperature
(4) Gas pressure
(5) Type of reaction gas
(6) Excitation state system

Table 3. CVD Method



This article will discuss various CVD systems based on the basic CVD principle and CVD technology applications:

(1) Various kinds of CVD units
(2) Filming conditions
(3) Various film properties

4. Tasks for Devices of 0.5 μm or Less

If all design rules, including the vertical direction, can be minified proportionally in device miniaturization, we can focus only on the thin film property, film thickness control, cleanliness and software, in addition to the miniaturization processing technology, in terms of the process.

However, in practice, proportional minification is unrealistic due to constraints imposed by circuit design, device design and layout design. Therefore, the aspect ratio of various device patterns tends to increase and, further, each element (passive or active) needs to be three-dimensional. Given these conditions, the development and tasks of CVD insulation film technology are described as follows:

(1) High derivative rate capacitance film formation

(2) Trench isolation embedding

(3) Interlayer evenness
    (3-1) Low temperature reflow
    (3-2) Inter Al layer film

(4) Low damage

(5) Film stress control

(6) Inter low derivative rate layer formation

Table 4. Insulation filming Method (CVD)

Method	Insulation film	Gas used
Normal pressure CVD	SiO_2 Doped SiO_2(PSG,BPSG,BSG) Al_2O_3 etc.	SiH_4, O_2, Alcoholate PH_3, B_2H_6 $AlCl_3$, $Al(CH_3)_3$
Reduced pressure CVD	SiO_2 Doped SiO_2(PSG,BPSG,AsSG) Si_3N_4 etc. High derivative rate film (Ta_2O_5, etc.)	SiH_4, SiH_2Cl_3, O_2, N_2O PH_3, B_2H_6, AsH_3, Alcoholate BCl_3, NH_3 $TaCl_5$, $Ta(OC_2H_6)_6$
Plasma CVD	SiO_2 Doped SiO_2(PSG,BPSG, etc.) Si_3N_4 (SiNxHy) SiON	SiH_4, O_2, N_2O, N_2 PH_3, B_2H_6, Alcoholate NH_3
Optical CVD	SiO_2 Si_3N_4 Ta_2O_6	SiH_4, O_2 NH_3 $Ta(OC_2H_6)_6$

Table 5. Basic Properties of Thin Film (1)

Film / Properties	SiO_2						
Reaction system	Normal pressure CVD	Normal pressure CVD	Reduced pressure CVD	Reduced pressure CVD	Plasma CVD	Plasma CVD	Optical CVD
Reaction gas	SiH_4-O_2	TEOS-O_2	SiH_4-N_2O	TEOS-O_2	SiH_4-N_2O	TEOS-O_2	SiH_4-O_2
Temperature (°C)	400~500	300~400	700~900	650~750	300~400	300~400	~300
Pressure (Torr)	760	760	0.4	0.4	0.4	8	5
Filming speed (nm/min)	200~300	200	5	10	50~300	700	30
Refraction factor	1.44	1.45	1.46	1.43~1.45	1.50	1.45	1.45
Stress (dyne/cm²)	1.1×10^9 tensile	1×10^9 tensile	1×10^9 compression	0.3×10^9 compression	1×10^9 compression	1×10^9 compression	$\sim1\times10^9$ compression
Step coverage	Bad	Very good	Very good	Very good	Bad	Good	Good
Crack resistance	Weak	Weak	Strong	Strong	Very strong	Very strong	Strong
Dielectric constant	4.0	4.0	4.0	4.0	4.0~4.8	4.0	4.0
Breakdown electric field(V/cm)	$8\sim9\times10^6$	$\sim10^7$	$\sim10^7$	$\sim10^7$	$3\sim8\times10^6$	——	$\sim10^7$

Table 6. Basic Properties of Thin Film (2)

Film / Properties	PSG (4 mol %)		BPSG		
Reaction system	Normal pressure CVD	Plasma CVD	Normal pressure CVD	Normal pressure CVD	Reduced pressure CVD
Reaction gas	SiH_4-PH_3-O_2	SiH_4-PH_3-N_2O	SiH_4-PH_3-B_2H_6-O_2	Alcoholate O_3	Alcoholate O_3
Temperature (°C)	400	300~400	400~300	~400	700
Pressure (Torr)	760	1.0	760	760	0.5
Filming speed (nm/min)	50~300	50~300	300~300	300	8
Refraction factor	1.42	1.46	1.46	1.43	1.46
Stress (dyne/cm²)	1×10^{9} tensile	$0.5\sim2.0\times10^{9}$ compression	0.8×10^{9} tensile	0.6×10^{9} tensile	0.4×10^{9} compression
Step coverage	Bad	Good	Bad	Very good	Very good
Reflow	Bad	Bad	Good	Very good	Very good
Breakdown electric field (V/cm)	5×10^{6}	5×10^{6}	6×10^{6}	6×10^{6}	6×10^{6}

Table 7. Basic Properties of Thin Film (3)

Film / Properties	Si_3N_4 (SiNH)			SiON
Reaction system	Reduced pressure CVD	Plasma CVD	Optical CVD	Plasma CVD
Reaction gas	SiH_4-NH_3	SiH_4-NH_3	SiH_4-NH_3	SiH_4-NH_3-O_2
Temperature (°C)	700~800	300~300	~300	~300
Pressure (Torr)	0.3	0.4	760	0.4
Filming speed (nm/min)	~10	30	~40	40~50
Refraction factor	1.85	1.85	1.87	1.85~1.75
Stress (dyne/cm²)	5×10^{9} compression	$5\sim7\times10^{9}$ compression	3×10^{9}	$1\sim2\times10^{9}$ compression
Crack resistance	Strong	Strong	Strong	Strong
Hardness (kg/mm²)	~2000	2000	—	2000~
Step coverage	Very good	Bad	Good	Bad
Dielectric constant	6.8	6.8	6.4	5~6
Breakdown electric field (V/cm)	4×10^{6}	5×10^{6}	4×10^{6}	5×10^{6}

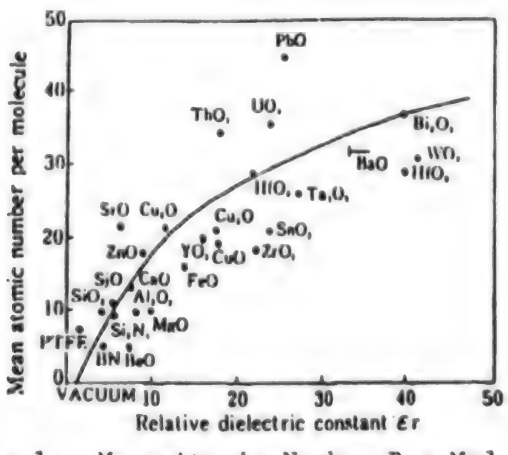


Figure 1. Mean Atomic Number Per Molecule and Measured Value of Relative Dielectric Constant

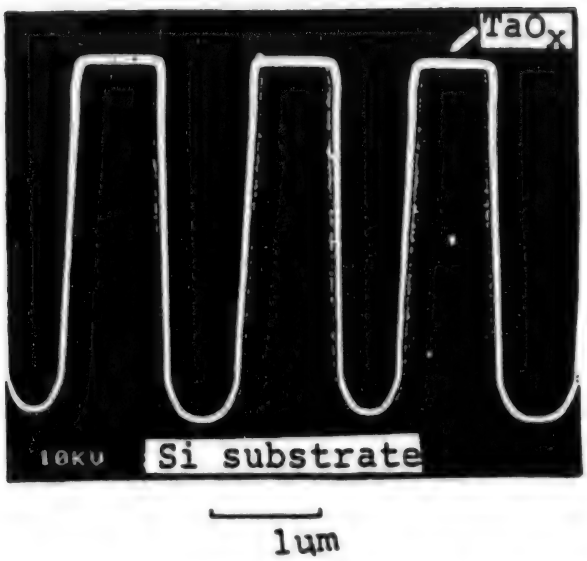


Figure 2. Cross Section SEM Photo of Tantalic Oxidized Film Clad Trench Groove

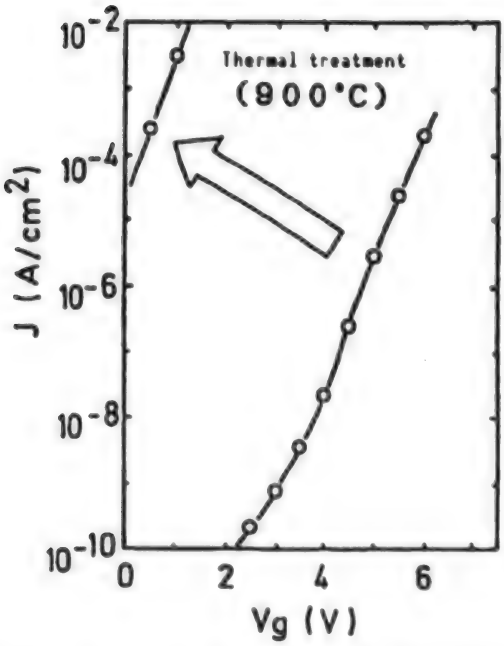


Figure 3. I-V Property of Tantalic Oxidized Film

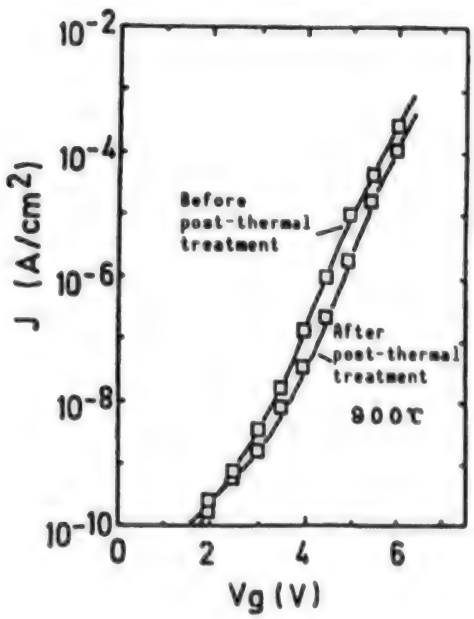


Figure 4. I-V Property of Tantalic Oxidized Film (Effect of surface nitriding)

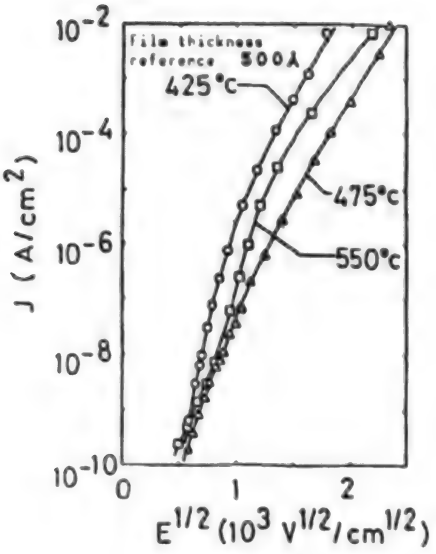


Figure 5. Current of Hafnium Oxidized Film--Electric Field Property

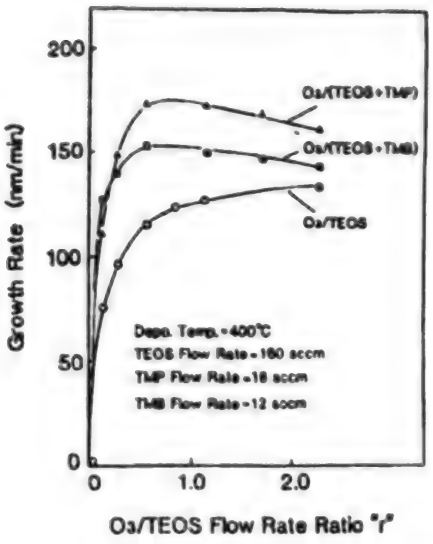
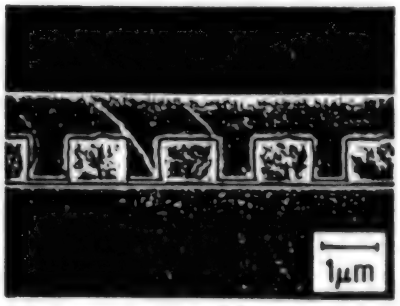
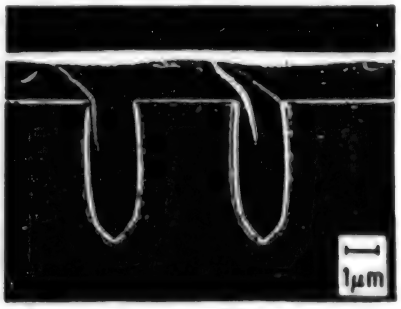


Figure 6. O_3 Quantity Dependency of Growth Speed in TEOS-O_3 Normal Pressure CVD



(a) Planartzation of Interlayer on Polycrystalline Silicon wring



(b) Deep Trench Filling

Figure 7. Cross Section SEM Photo of BPSG Film Deposited by TEOS-03 Normal Pressure CVD

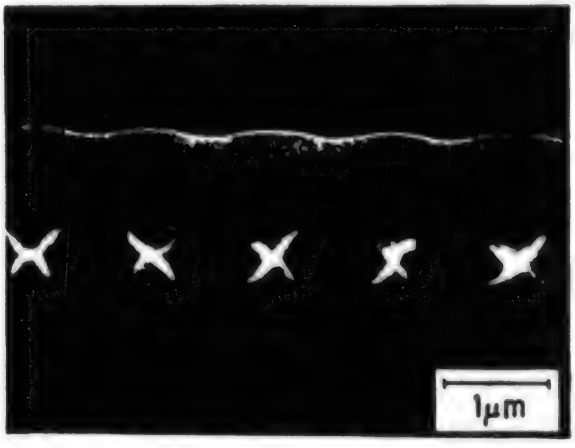


Figure 8. Cross Section SEM Photo Planarized With TEOS-O_3 Normal Pressure CVD

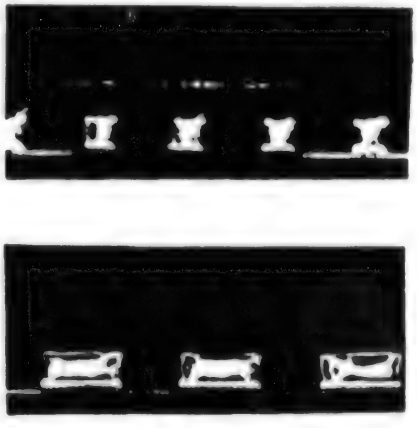


Figure 9. Cross Section SEM Photo Planarized With Bias ECRCVD

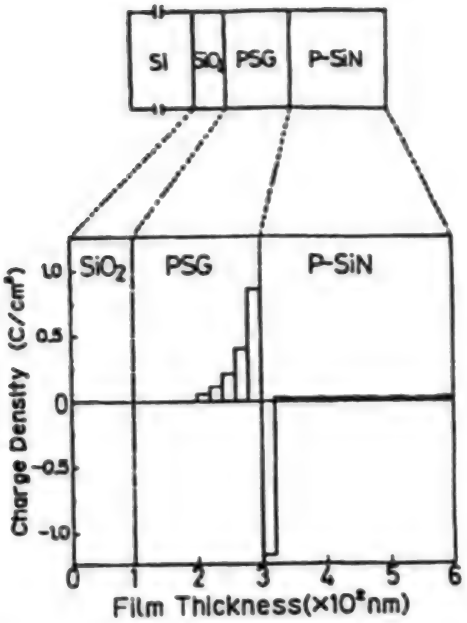


Figure 10. Charge Density After Plasma CVD Nitrization Filming

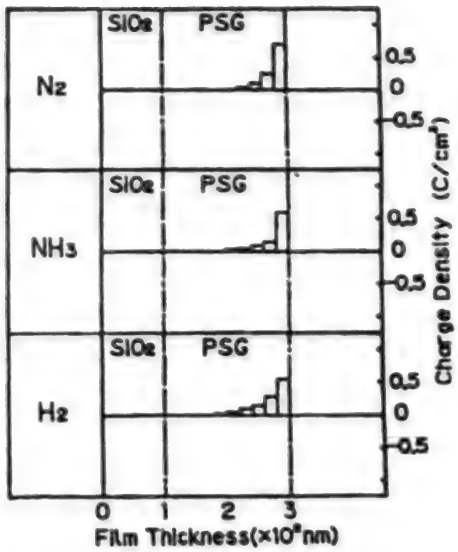


Figure 11. Difference of Charge Density Depending on Reaction Gas

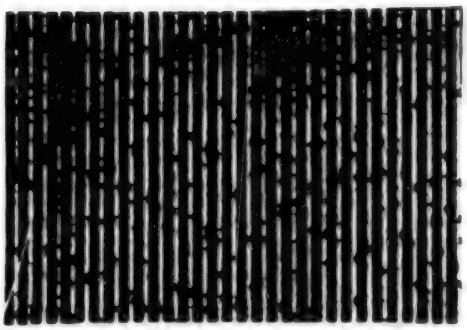


Figure 12. Optical Microscopic Photo Showing Aluminum Disappearance

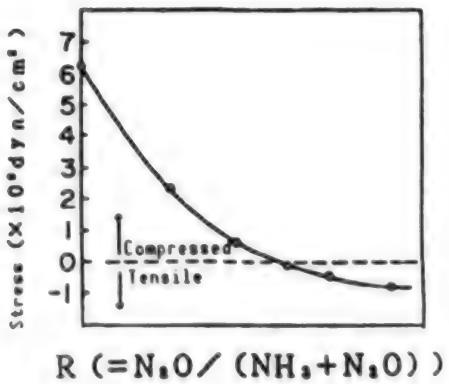


Figure 13. SiON Film Stress Dependency on N_2O Gas Flow

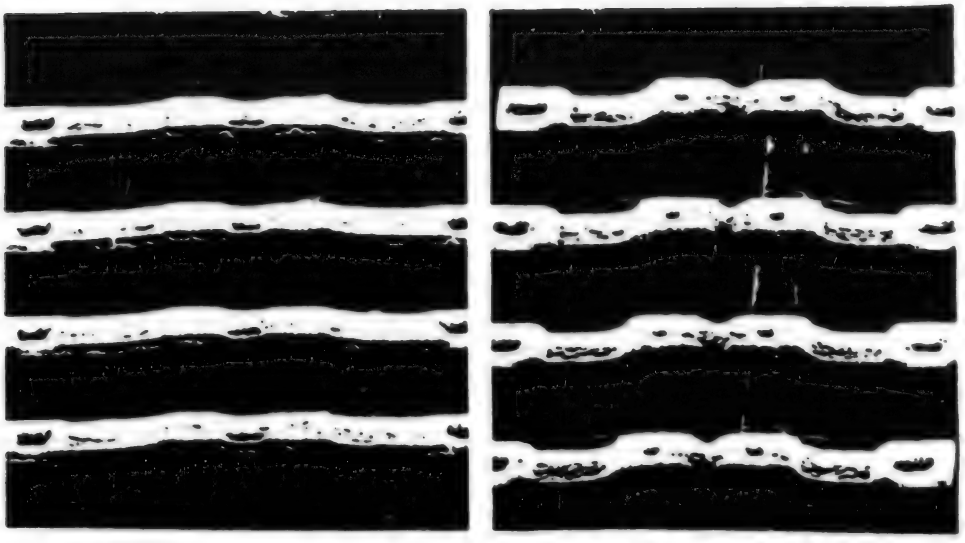


Figure 14. SEM Photo of Aluminum Wiring

5. Future Prospects

The emerging insulation film CVD technology can be expected to focus on the following in view of the problems facing and the prospects for mass production of CVD technology.

(1) Mechanism clarification and simulation

(2) Embedding/high planarization

- Growth method: unit, gas, etc.
- Composite process: combination with coated film

(3) Software

- Low damage
- Low temperature

(4) High controllability

- In-process monitoring

(5) Clean processing

- Particles
- Impurities

(6) Large diameter

- Pieces format

(7) Automation

- In-line

(8) Flexibility

- Pieces format
- Multichamber

(9) Throughput

References

1. P.J. Harrop and D.S. Campbell, THIN SOLID FILMS, Vol 2, 1968, p 273.

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